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An Optimized Multiphase Bridgeless SEPIC Converter for High-Power Applications with Distributed Thermal Management and Enhanced Power Factor Correction

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KEYWORDS

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Bridgeless SEPIC Converter,
Intra-phase Interleaving,
Power Factor Correction,
Total Harmonic Distortion,
PID Control,
Thermal Management.

ABSTRACT

This paper presents the design and implementation of an optimized multiphase bridgeless SEPIC converter for high-power applications, such as fast-charging systems in electric vehicles (EVs), renewable energy interfaces, and industrial drives where the system operates under stable load conditions. An intra-phase interleaving technique is employed; wherein multiple switching legs are interconnected within the same phase to enhance thermal distribution and reduce component stress by equalizing current paths. This system combines a three-phase interleaved power factor correction (PFC) rectifier and a multiphase interleaved SEPIC converter, both controlled by PID controllers that contain signals with a 180-degree phase shift within each phase. High-fidelity simulation environment demonstrates low conduction ripple and a total harmonic distortion (THD) of less than 3%, as well as stable output voltage regulation of up to 800V at 5kW. The proposed design ensures thermal balance and a stable DC output under constant load, thereby improving system reliability and extending operational lifespan. These results provide a foundation for future investigations under dynamic load conditions.

1. INTRODUCTION

With the increasing pace of worldwide decarbonization of transportation and energy generation, the design of strong and efficient power converting systems has gained importance as a new pillar of the contemporary energy infrastructure. Electric vehicle (EV) charging systems, photovoltaic (PV) interfaces, and industrial automation applications not

only call upon capability at high power levels but also must meet high power quality, low electromagnetic interference (EMI), and temperature stability requirements [1]. The loading condition on these systems is usually steady-state, and an opportunity to design converters optimizing steady-state operation with low total harmonic distortion (THD) and better heat management exists [2] . A topology that is popular in applications that need a non-inverting output or in applications that need wide flexibility to handle wide input voltages is the Single-Ended Primary-Inductor Converter (SEPIC) [3]. Nevertheless, regardless of these benefits, SEPIC converters have certain shortcomings when applied to larger-scale applications in kilowatts, which include higher conduction losses, component stress, and fluctuating heat distribution [4]. In an attempt to curb these problems, different strategies have been proposed by the researchers, such as interleaved operation and bridgeless rectification, that play different roles in enhancing the areas of efficiency and reliability [5].

Multiphase interleaving, in which more than one converter phase is connected and driven with interleaved control signals, is familiar as a way to minimize current ripple and more evenly share power processing among different components, which does not simply increase the system efficiency but also makes the components smaller and less thermally stressed [6]. Recently, finer current division between stages since phases is employed by the use of intra-phase interleaving. In this, a converter single stage may have several switching legs per phase, and the phase current is common to all legs, thereby enabling even greater current balance and enhanced thermal consistency. These methods apply especially to high-frequency, high-power converters. Simultaneously, there has also been the growth in adoption of bridgeless topologies, that is, removal of traditional input diode bridges, as a method of power factor correction (PFC) [7] [8]. Bridgeless PFC rectifiers reduce the conduction paths hence causing less power loss hence improving the conversion efficiency [9]. By combining with SEPIC-based converters the designs provide an attractive step-up/step-down capability and high input power quality. These designs are very useful in three-phase designs [10]. It is also equally important to apply the control strategies used to control such complex converter systems. Proportional-Integral-Derivative (PID) controller has continued to be one of the favorite industrial controllers because it is simple and effective when the desired voltage and current control is required. Creating independent PID controllers in every interleaved leg of a converter phase allows the designer to have a finely grained control and improves the dynamic response [11] [12]. Moreover, phase shifts(as a 180-degree phase shift between intra-phase legs signals) have also been demonstrated to reduce the ripple and harmonics, assist in improving overall waveform quality and power factor.

A comprehensive literature review is provided in Section II, which comes after the structure of this paper. The literature review in the Section II contains the details of, making particular focus on the development and drawbacks of the current designs of converters. In Section III, the architecture of the proposed system is described, and component selection and interleaving approach have been detailed. The structure of control and a methodology of simulation are explained in Section IV. In section V, the components design and analysis are covered and in Section VI & VII, the simulation modeling as well as results are reported and analyzed to show key performance indicators. Lastly, Section VIII will end the study with a conclusion on the prospects of further research, especially on how to design it under dynamic loading conditions.

2. LITERATURE REVIEW

Advances in high-power SEPIC converters have recently centered a lot on minimizing current ripple, enhancing thermal characteristics and even the efficiency of the whole system [13]. Interleaving methods have been very effective in this aspect and have reduced the input and output current ripple significantly, leading to the enhanced electromagnetic compatibility [14]. Since interleaving of converter phases can push the consumption in each one to a more constant value, the passive components have to face less stress and the system can be more reliable [15]. The other most effective technique that has been developed to minimize conduction losses is bridgeless topologies. Such arrangements avoid the classic input diode bridge, thus minimizing the conduction paths in use. The effect is that the conversion efficiency increases and power losses decrease [16]. Where bridgeless rectification is used in

combination with SEPIC converter implementation, the resulting system has the advantages of both a flexible converter, and the improved input power quality, especially in three-phase applications [17] [18].

Despite the definite benefits that both interleaving and bridgeless topologies provide, the implementation using both of them remained unexplored to a certain extent [19].The historic methods have been primarily concerned with the interleaving between independent stages of converters. Conversely, within-phase interleaving is segmenting the phases of each converter into several identical parallel switching legs. This sophisticated design enhances sharing current and thermal balance per individual phases, which is very advantageous in high-frequency and high-power contexts [20]. The intra-phase interleaving concept is also considerable advantageous in thermal management. The more equalized distribution of the heat generation along the internal structure of the converter lowers the demand for large heat sinks and improves the overall thermal input [21] [22]. This is vital in applications where the application is run under continuous loading so as to give the application an early side in cases of high-powered applications like the electric vehicle chargers, renewable energy converters, and industrial drives.

These advanced power converters also rely on control strategies that are very crucial in their successful operation. The Proportional-Integral-Derivative (PID) controller is one of the most popular solutions among approaches that are currently available. It is also very simple to operate, highly adjustable, and has high efficiency that lends it sufficiently to high power voltage and current control [23]. Using personal PID controllers in each of the interleaved legs will allow modular control, better transient response, and increase the overall stability of this signal [24]. Although the area has advanced, a complete consensus on all three operations, including intra-phase interleaving, modular PID regulation, and bridgeless SEPIC architecture, has not been achieved. This opens the possibility of coming up with a uniform system that embraces the strengths of these strategies and enhances performance in a steady state of loading. The given proposal fills in this gap by offering a high-efficiency, thermally balanced, and power-quality converter architecture.

3. DESIGN AND ARCHITECTURE OF THE MULTIPHASE BRIDGELESS SEPIC CONVERTER

It is proposed that the system converter can solve the shortcomings of the traditional single-phase and phase-interleaved converters through the incorporation of a three-phase bridgeless rectification output coupled with an interleaved SEPIC converter with intra-phase current sharing. The system uses steady-state load working, and this is aimed at high power applications that include EV charging and industrial energy conversion. The architecture is comprised of three principal modules (i) three-phase AC input source, (ii) bridgeless power factor correction (PFC) rectifier, and (iii) Multiphase SEPIC with intra-phase interleaving converter as shown in Fig.1.

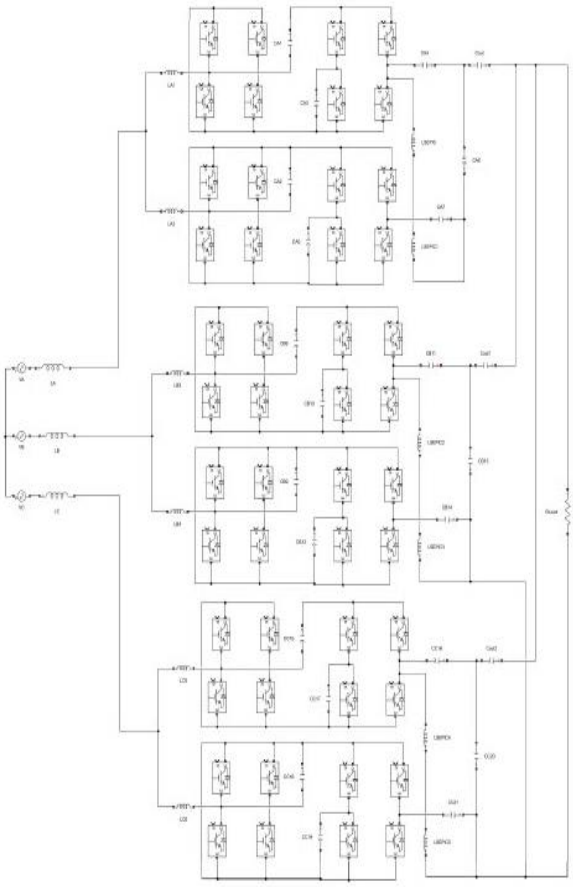


Fig.1. Multiphase Bridgeless SEPIC Converter Circuit Diagram

The processing of each stage of the input occurs on a separate leg of the rectifier, so there is no conventional full-bridge diode configuration, and the losses associated with conduction are correspondingly minimized. The rectified DC is then passed to the SEPIC stage, which has two or more interleaved legs per phase and which

operates with a 180- degree phase shift to minimize the current ripple and to allow better thermal balance. The energy is conducted within a series-coupled capacitor-inductor-capacitor path in both SEPIC legs, permitting both step-up and step-down conversion. Several legs per phase are interlaced, so the total current is shared among more components, reducing current density on any given part of the circuit, and allowing the entire aggregate to be more easily cooled.

The two SEPIC legs (comprising four separate legs) each have their own PID controller and are driven independently in order that the level of regulation and current balance is achieved within a precise degree of control under all operating conditions. Each of these controllers has its own error signal using feedback in the output voltage sensors and current sensors inside each leg. A 180-degree shift of phase between intra-phase legs is done by use of a synchronous PWM generation technique that shifts the pulses to generate switching without affecting the timing throughout the system. Fig. 1 gives the schematic of the proposed converter. It shows the configuration of the bridgeless rectifier, integrated with an interleaved SEPIC stage. The component value and switching frequencies can be determined given desirable power output levels, efficiency requirements and thermal design limits. This architecture structure enhances conversion efficiency in addition to saving space on the filtering components, heat sinks, thus it allows a smaller and more heat-balanced converter which performs well in high-power applications. The strategies related to the control will be discussed further, and the simulation results determining the performance of the proposed system will be given in further sections in detail.

4. CONTROL STRATEGY

To ensure high power factor correction, steady output regulation, as well as to balance thermal loading, a strong dual-loop control approach is used in the proposed multi-phase bridgeless SEPIC converter system. The control structure is outlined, incorporating two feedback loops. one the outer loop, is a voltage regulation loop, and the other is the inner loop, a current control loop, and both are executed via a discrete-time PID control. The control is implemented on a per-phase basis with the intra-phase interleaving, so that the three different phases become synchronized.

A. Grid Synchronization with Phase-Locked Loop (PLL)

A Phase-Locked Loop (PLL) is incorporated at the rectifier front end to measure the grid voltage phase angle correctly, as shown in Fig.2. This makes sure the reference current carried out as Power Factor Correction (PFC) is in-phase with the input voltage thus meaning that near unity power factor operation is possible. The angular position θ(t) is supplied via the PLL and generates the reference currents $i_A^*(t)$, $i_B^*(t)$, and $i_C^*(t)$ as;

$$i_{abc}^*(t) = I_{ref}.\sin(\omega t + \emptyset) \quad (1)$$

Where

I_{ref} = derived from the DC output voltage error
$\emptyset$ = phase shift synchronized using PLL

B. Dual loop PID control

The PID Control implementation in both rectifier and SEPIC Converter ensures the external voltage regulation feedback signal contrasts the output voltage V_{out} and the reference with V_{ref} and acts as a current reference generator I_{ref}. This is followed by an inner current loop, and this is the current that follows sinusoidal reference current values per phase. These are set to produce the best dynamic performance. Such gains are tuned independently between the controllers (voltage and current) on each phase, as shown in Fig.3.

Voltage error: $e_v(t) = V_{ref} - V_{out}(t)$ (2)

Current error: $e_i(t) = i_{in}^*(t) - i_{in}(t)$ (3)

PID Control Law (in generalized form):

$$u(t) = K_p e(t) + K_i \int e(t)\,dt + K_d \frac{de(t)}{dt} \quad (4)$$

Where

$K_p = proportional\ gain$
$K_i = integral\ gain$
$K_d = derivative\ gain$

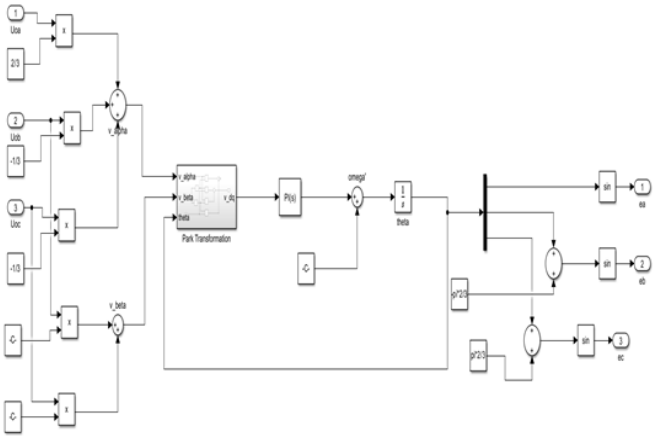


Fig.2. PLL (Phase-Locked Loop) Control of Rectifier

C. PWM Signal Generation and Intra-Phase Interleaving

The PWM signals are modulated by the controller output u(t) to turn on the IGBTs in the two SEPIC legs. To reduce ripple and to spread thermal stress equally on the three phases (A, B, C), drives are fed 120-degree phase-shifted PWM signals. Intra-phase interleaving is utilized between the interleaved legs of each phase (e.g., A1, A2); their PWM signals are shifted by 180 degrees at a phase.

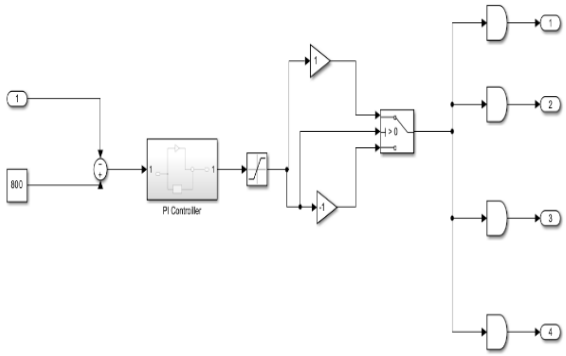


Fig.3. PID Control of SEPIC Converter

5. COMPONENTS DESIGN & ANALYSIS OF MULTIPHASE BRIDGELESS SEPIC CONVERTER

The power electronic components have to be accurately designed to reach the desired performance, like the unity power factor, low total harmonic distortion (THD), and high efficiency in the high-power converters. The considerations to select the components in the proposed three-phase interleaved bridgeless SEPIC topology include steady-state equations, ripple current limitations, thermal distribution, and switching characteristics.

The design computations are undertaken on the basis of the continuous conduction mode (CCM), which is ideal for high-power operation and minimizes core and copper losses. The specifications of the proposed system are shown in the below Table-I & Table-II.

A. Three-Phase PFC Intra-Phase Interleaved Bridgeless Rectifier

By considering the specifications of table-I which is shown below, rectifier parameters have been determined to fulfill high power factor correction, low input current ripple, and useful intra-phase interleaving to realize good AC to DC conversion with high power applications.

Three-phase Line-to-Line RMS Input Voltage

$$(V_{LL}) = 400\ \text{V} \qquad (5)$$

(a) Phase Voltage (RMS)

$$V_{ph} = \frac{V_{LL}}{\sqrt{3}} = \frac{400}{\sqrt{3}} = 230.94\text{V} \qquad (6)$$

(b) Peak of Phase Voltage

$$V_{ph-peak} = V_{ph} \cdot \sqrt{2} = 326.60\text{V} \qquad (7)$$

(c) Input line current = 7.38A (8)

The value of 7.38 A is chosen because of Safe operating limits of the IGBTs, so that intra-phase interleaving can be practiced to reduce the stress and current distribution to ~4.26A RMS per phase wire windings (post interleaving).

$$P_{in} = \sqrt{3} \cdot V_{LL} \cdot I_{LL} \cdot \cos(\emptyset) \qquad (9)$$

$$= \sqrt{3} \cdot 400 \cdot 7.38 \cdot 0.99$$

$$= 5060\ \text{W}$$

Table-I. Specifications of Three-Phase Bridgeless PFC Rectifier

S.No	Design Variables	Values
1	AC Input Voltage (RMS)	400V
2	Duty Ratio (D)	0.396
3	Switching frequency	50KHz
4	Inductance (L_{x1} , L_{x2} ,) → x = A,B,C	$2mH$
5	Capacitance (C_{x1} , C_{x2} ,) → x = A,B,C	3 μF

(d) Rectifier Output DC Voltage

$$V_{DC} = \frac{3\sqrt{2}}{\pi} \cdot V_{LL} \approx \frac{3\sqrt{2}}{3.1416} \cdot 400 \approx 540.7\text{V} \qquad (10)$$

(e) Total Input Current (3-Phase)

$$I_{in\_total} = \frac{P_{in}}{V_{LL}} = \frac{5060}{400} = 12.65\text{A} \qquad (11)$$

(f) Current Per Phase

$$I_{in\_phase} = \frac{I_{in\_total}}{3} = \frac{12.65}{3} = 4.21\text{A} \qquad (12)$$

(g) Output Current of Rectifier

$$I_{out\_rectifier} = \frac{P_{in}}{V_{DC}} = \frac{5060}{540.7} = 9.35\text{A} \qquad (13)$$

(h) Design of Interleaved Inductors

The design ripple is assumed to be 20% and this is a typical design trade-off giving a good dynamic response and thermal balance.

$$\Delta I_L = 0.2 \cdot I_{in\_phase} = 0.2 \cdot 4.25 = 0.85\text{A} \quad (14)$$

$$\text{Switching frequency } (f_{sw}) = 50\text{KHz} \quad (15)$$

Time:

$$T_s = \frac{1}{f_{sw}} = \frac{1}{50*10^3} = 20\mu s \quad (16)$$

Inductance Required Per Phase:

$$\text{L} = \frac{V_{ph-peak} \cdot D \cdot T_s}{\Delta I_L} \quad (17)$$

(i) Duty Ratio of Three-Phase Bridgeless PFC Rectifier

The ratio of the duty of the bridgeless PFC rectifier is programmed to change in a sinusoidal way with the input AC waveform. Under the full input voltage of 326.6 V (400 V L-L RMS), the duty ratio decreases to about 0.396, which is an optimum conversion ratio to operate as a boost converter. This has the advantage of low conduction losses and good thermal characteristics over and above producing the required output of 540.7 V with near-unity power factor.

$$\text{D} = 1\text{-} \frac{V_{ph-peak}}{V_{DC}} \quad (18)$$

$$\text{D} = 1\text{-} \frac{326.60}{540.7} = 1\text{-}\ 0.6039 \approx 0.396$$

$$\text{L} = L_{per\_ph} \frac{326.60 \cdot 0.396 \cdot 20*10^{-6}}{0.85} = 3.0431\text{mH} \quad (19)$$

$$L_{leg}=L_{x1}= L_{x2} = \frac{3.0431\text{mH}}{2} \text{ (2 legs per phase)} = 1.52\text{mH} \quad (20)$$

Where

x = A, B, C (for three phases of PFC Rectifier with two legs each)

(j) Design of Capacitance

In order to get low ripple and stable DC-link voltage on the bridgeless interleaved PFC rectifier, a ripple voltage of 2% of the output voltages is required. This gives ideal power factor correction and downstream converter viability.

$$V_{DC} = 540.7\text{V}$$

$$\Delta V_{DC} = 2\% \cdot V_{DC} = 0.02 \cdot 540.7 = 10.81\text{V} \quad (21)$$

$$I_{DC} = \frac{P_{out}}{V_{DC}} = \frac{5000}{540.7} \approx 9.24\text{A} \quad (22)$$

$$I_{phase} = \frac{I_{DC}}{3} = \frac{9.24}{3} \approx 3.08\text{A} \quad (23)$$

(k) Output Current Per Leg (2 Legs per Phase)

$$I_{leg} = \frac{I_{phase}}{2} = \frac{3.08}{2} = 1.54\text{A} \quad (24)$$

(l) Capacitance per leg for boost PFC rectifier

$$C_{leg} \geq \frac{I_{leg}}{f_{sw} \cdot \Delta V_{DC}} \quad (25)$$

$$C_{leg} \geq \frac{1.54}{50\times10^3 \cdot 10.8} \approx \frac{1.54}{540{,}000} \approx 2.85\mu F$$

Therefore, $C_{leg} = C_{x1} = C_{x2} = 2.85\mu F$ (26)

Where,

x = A, B, C (for three phases of PFC Rectifier with two legs each)

A. Multiphase Interleaved SEPIC Converter Components Design

The component values as shown in Table-II are computed in terms of duty cycle, power level, and 20% ripple requirements, and thus there is balanced current sharing and limited output ripple between interleaved legs.

TABLE-II. SPECIFICATIONS OF MULTIPHASE SEPIC CONVERTER

S.No	Design Variables	Values
1	SEPIC DC Input Voltage	540.7V
2	Duty Ratio (D_{SEPIC})	0.597
3	Switching frequency	50KHz
4	Inductance (L_{x1} , L_{x2} ,) → x = A,B,C	3mH
5	Capacitance (C_{x1} , C_{x2} ,) → x = A,B,C	4.7 μF
6	Output Capacitance(C_{out})	2200 μF
7	Load Resistance (R_L)	128Ω
8	Output Voltage (V_{out})	800V
9	Output Power (P_{out})	5KW

(a) SEPIC Voltage Gain

$$V_{out} = \frac{D_{SEPIC}}{1-D_{SEPIC}} \cdot V_{in} \ (\therefore V_{in} = V_{DC}) \quad (27)$$

$$D_{SEPIC} = \frac{V_{out}}{V_{out}+V_{in}} = \frac{800}{800+540.7} = \frac{800}{1340.7} \approx 0.597 \quad (28)$$

(b) Output Load Current:

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{5000}{800} = 6.25\text{A} \quad (29)$$

The current per phase is;

$$I_{phase} = \frac{6.25}{3} = 2.083\text{A} \quad (30)$$

The current per interleaved leg is;

$$I_{leg} = \frac{2.083}{2} = 1.0415\text{A} \quad (31)$$

(c) Design of SEPIC Inductance:

$$\text{L} = \frac{V_{in} \cdot D}{f_{sw} \cdot \Delta I_L} \quad (32)$$

$$\Delta I_L = 0.2 \cdot 6.25 = 1.25\text{A} \quad (33)$$

$$\text{L} = \frac{540.7 \cdot 0.597}{50\times10^3 \cdot 1.25} = 5.1647\text{mH} \quad (34)\ L =$$

$$L_{per\ phase} = \frac{L_{per\ leg}}{2} = \frac{5.1647\times10^{-3}}{2} = 2.582\text{Mh} \quad (35)$$

Assuming 20% ripple for inductance design and the interleaved SEPIC converter inductance value of 2.58mH/per leg has been selected to provide low ripple current in light of high-voltage, high-power applications and enhanced thermal and EMI needs.

(d) Design of SEPIC Capacitance

$$C_{leg} = \frac{I_{out} \cdot D_{SEPIC}}{f_{sw} \cdot \Delta V} \quad (36)$$

$$\Delta V = 0.02 \cdot 800 = 16\text{V} \quad (37)$$

$$C_{leg} = \frac{6.25 \cdot 0.597}{50\times10^3 \cdot 16} = 4.664\mu F \approx 4.7\mu F \quad (38)$$

$$C_{per\ phase} = 2 \times C_{leg} = 2\times 4.664 = 9.328\mu F \quad (39)$$

(e) Output Capacitance Calculation

$$C_{out} = 2200\ \mu F \quad (40)$$

It is desired to reach a high-power operation and good output voltage stability, as well as minimal output voltage ripple which makes the output capacitance of the SEPIC converter to be chosen as 2200 μF. Although the theoretical value of standard ripple-based calculation is lower, higher capacitance has been selected based on transient response, load step handling, and to achieve distributed thermal management under high load conditions. It is a convenient design decision helping to guarantee the reliability and better performance of the system, which converges with the goal of the proposed high-power, better operational stability and an optimized multiphase SEPIC converter architecture.

6. SIMULATION MODELING OF THE MULTIPHASE BRIDGELESS SEPIC CONVERTER

The proposed topology of the converter is designed in Simulink of high-fidelity environment , through discrete time simulation as shown in Fig.4. The AC three-phase input and bridgeless interleaved PFC rectifier and interleaved SEPIC converter are designed in discrete form with the simulator, are shown in Fig.5 and Fig.6, respectively. Intra-phase interleaving is applied on each of the legs of the rectifier, and the control of the rectifier is achieved using PID blocks independent of each other, tuned at a unity power factor, which is almost utilized. Likewise, the SEPIC stage takes phase-shifted PWM and individual PID voltage control per interleaved leg.

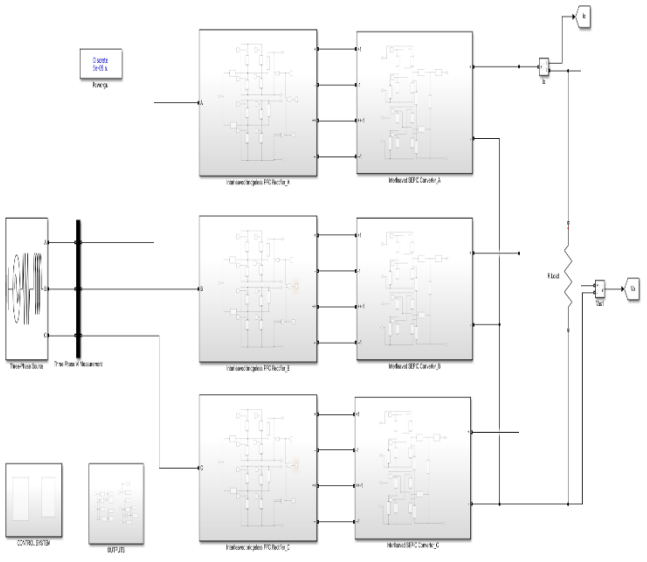


Fig.4. Simulation Setup of Multiphase Bridgeless SEPIC Converter

The generation of the gate pulses is based on 120 phase-shifted carrier-based generation of PWM signals, which have to be applied individually to each phase. Interleaving provides implied thermal balancing, and hence, no explicit thermal process modeling is present during simulation.

The THD of the input and output voltage regulation, phase currents, and power factor are monitored during nominal-load steady-state operation using key measurement blocks. The efficacy of the proposed structure in minimizing the thermal bottleneck conditions and subsequent improvement of power quality was conclusively evidenced in the quantitative nature of the monitored outputs during the simulation process.

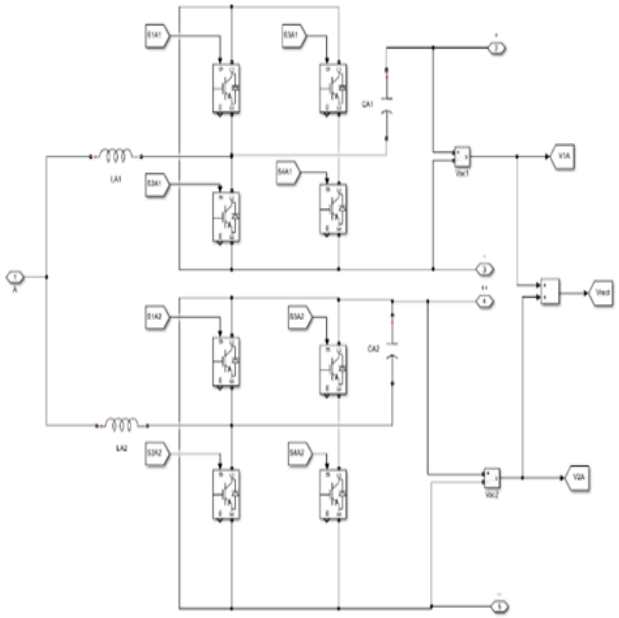


Fig.5. Intra-Phase Interleaved PFC Rectifier

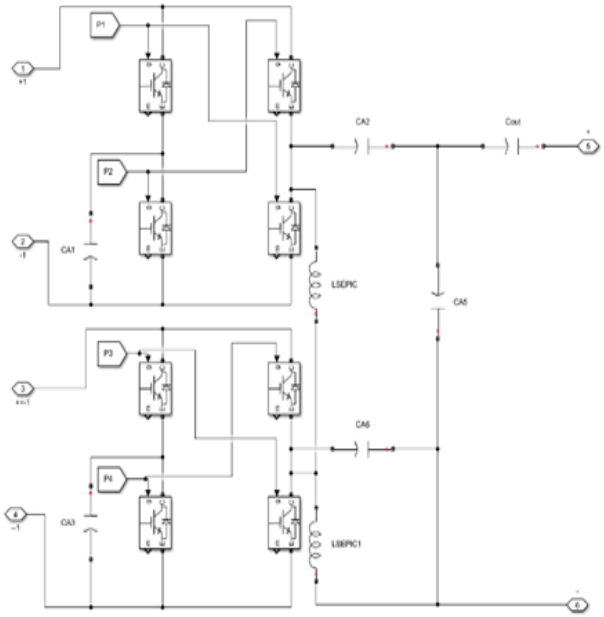


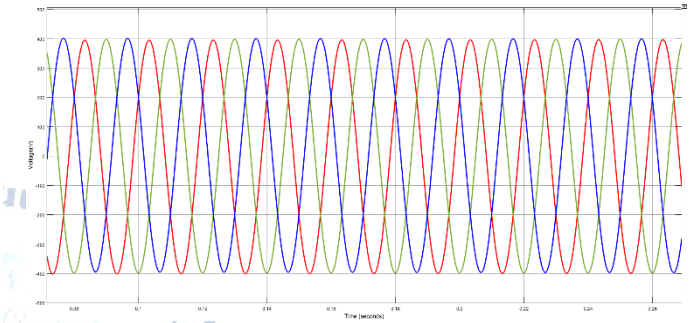
Fig.6. Intra-Phase Interleaved SEPIC Converter

The results of the simulation setup, covering various performance parameters such as output voltage regulation, power factor, and total harmonic distortion (THD), are presented in the subsequent section in detail.

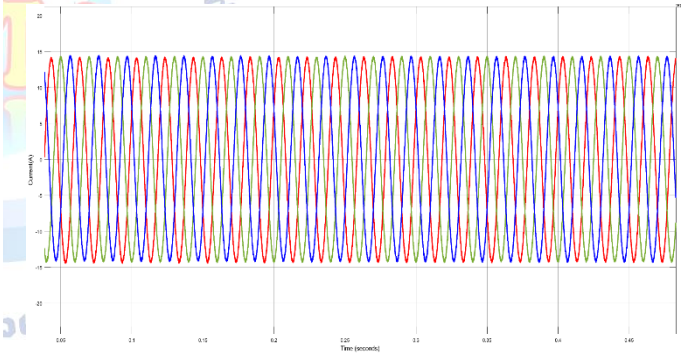
7. RESULTS AND DISCUSSION

In order to confirm the operation of the proposed three-phase intra-phase interleaved bridgeless SEPIC converter at high power levels, the converter was simulated in high-fidelity environment in the steady-state regime. The simulation was conducted to confirm that the converter could meet high power factor correction (PFC), low total harmonic distortion (THD), and increased thermal distribution with no need of using extra cooling.

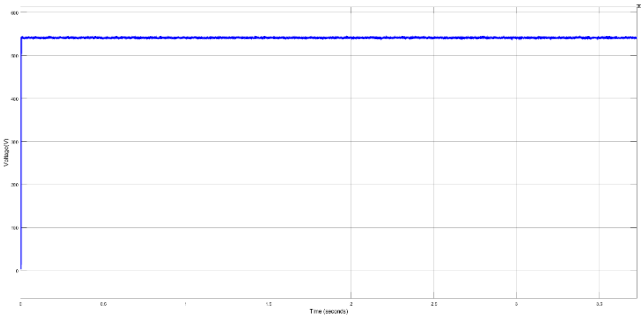
A 3-phase and 400 V AC 50 Hz input was tested the system, from which the following results were obtained and are shown in the Fig.7(a),7(b), and 7(c). The use of a bridgeless rectifier stage successfully avoided the losses that were due to diode bridge applications and facilitated the enhancement of symmetrical input currents between phases. Intra-phase interleaving was used for each leg of the rectifier and SEPIC stages, to ease peak current stress and more evenly distribute a heat load among all the switching devices.



(a)



(b)

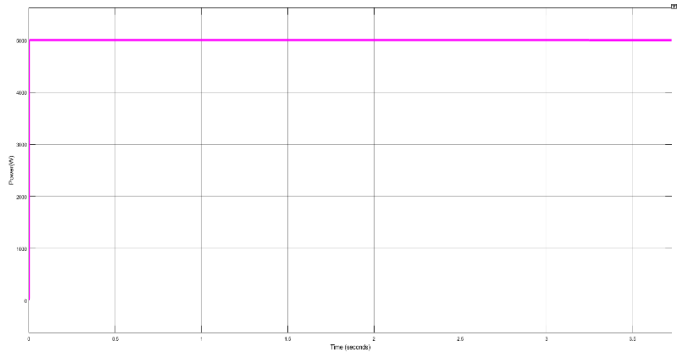


(c)

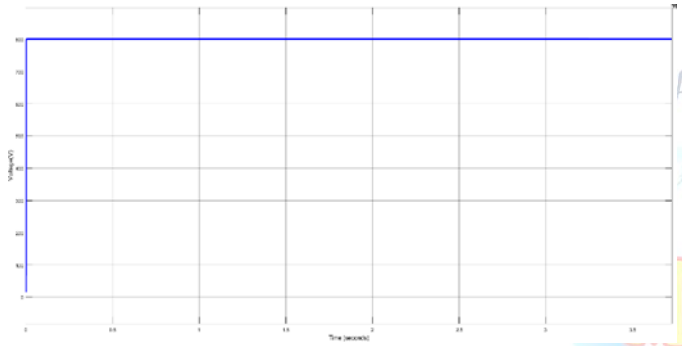
Fig.7. Three-Phase Bridgeless Intra-Phase Interleaved PFC Rectifier: (a) Input Voltage, (b)Input Current, and (c)Output Voltage Waveforms

SEPIC converter stage, working at a duty ratio of 0.597 and switching frequency of 50 kHz, continues to provide a regulated output voltage of about 800 V with a 5kW load as shown in Fig.8(a) and 8(b). It enhanced the

performance of the voltage ripple because of using the interleaved SEPIC legs which lowered the electromagnetic interference (EMI). A PID controller was used to control the PFC and the output voltage in order to maintain the rapid dynamic response and small steady state error.



(a)



(b)

Fig.8. Multiphase Interleaved SEPIC Converter Waveforms of: (a)Output Voltage, and (b)Output Power

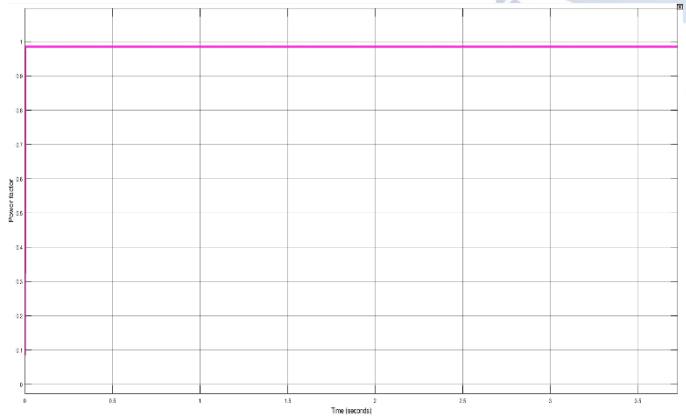


Fig.9. Power Factor at Rectifier

The simulation outcome shows the power factor of almost unity (0.98), and THD of <3% are shown in Fig.9 and Fig.10. respectively, and the DC output voltage under full load is highly stabilized. Due to interleaving, the thermal stress at every phase leg was balanced, which implicitly enabled thermal management. These results confirm the feasibility of the proposed topology when it comes to high-power systems of applications, including power chargers of electric vehicles and industrial power supplies.

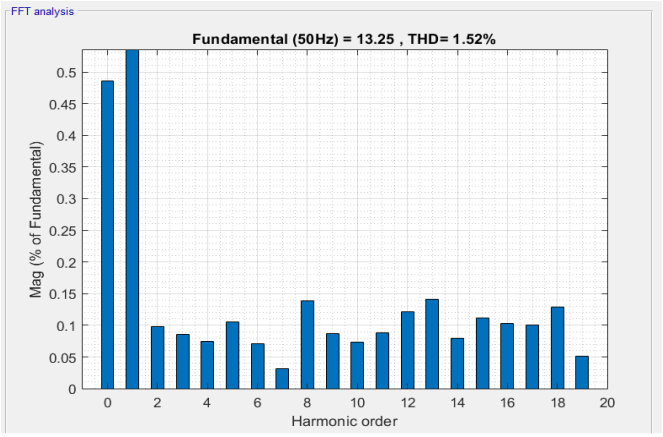


Fig.10. Harmonic Current Spectrum of Input Current

8. CONCLUSIONS

This paper has presented a new three-phase intra-phase interleaved bridgeless single-ended positive-input converter to solve the problems of high-power applications, where better power factor correction, better thermal characteristics, and small size are needed. As the traditional diode bridge is removed and replaced with phase-wise interleaving in the rectifier and SEPIC section, conductive losses are minimized, thermal coupling is improved, and the architecture of controls can be simplified as only PID controllers are used instead. The converter architecture proved to be an optimized solution that has kept pace with the changes of the electric mobility and the industrial DC loads, providing a common denominator power quality and system robustness. Intra-phase interleaving integration is involved in thermal management, which is able to operate the converter under continuous high-power stress with no additional complexity. This paper provides the basis of future research in modular, scalable, high-efficiency power conversion systems. Implementation of additional hardware, digital control strategies, and adaptive thermal sensing to strengthen the reliability of systems and real-time control may be studied further.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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