



Approximate Reverse Carry Propagate Adder for Energy Efficiency DSP Applications

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KEYWORDS	ABSTRACT
Accuracy, approximate adder, digital signal processing (DSP), energy efficient, reverse carry propagate adder (RCPA).	<i>The Reverse Carry Propagate Adder (RCPA) introduces a novel approach to addition by reversing the direction of carry propagation, allowing the carry signal to move from the most significant bit (MSB) to the least significant bit (LSB). This method enhances stability under delay variations by assigning higher significance to the carry input than the output carry. Three implementations of the Reverse Carry Propagate Full- Adder (RCPFA) cell is proposed, each optimized for different trade-offs in delay, power, energy efficiency, and accuracy. Additionally, RCPA can be integrated with traditional forward carry adders to form hybrid adders with adjustable accuracy levels. Simulation results using HSPICE in 45-nm CMOS technology indicate that RCPA-based hybrid adders achieve 27% reduction in delay, 6% lower energy consumption, and a 31% improvement in the energy-delay product compared to conventional approximate adders. Furthermore, the structure demonstrates greater resilience to delay variations, making it highly suitable for energy-efficient applications. The effectiveness of RCPA is validated in JPEG compression's discrete cosine transform (DCT) and finite-impulse response (FIR) filtering, achieving 60% and 39% energy savings, respectively. These findings establish RCPA as a promising solution for low-power digital signal processing (DSP) applications, particularly in image and audio processing, embedded systems, and energy-efficient computing.</i>

1. INTRODUCTION

Approximate Reverse Carry Propagate Adder (ARCPA) designed using pass transistor logic in a cutting-edge approach aimed at enhancing energy

efficiency in Digital Signal Processing (DSP) applications. Traditional adders mainly prioritize accuracy and speed, but this often comes at higher power consumption, which leads to critical constraints at

modern DSP applications. The combination of approximate computing techniques with pass transistor logic makes the ARCPA a powerful candidate for next-generation DSP architectures. The power consumption and energy efficient are the key goals of this adder for portable devices. Increase in speed can lead to the high cost of power consumption. One of the approaches to improve both the power and speed is to sacrifice the computation exactness. This approach, which is approximate computing, may be used for the applications where some errors may be tolerated.

Adder blocks are the main components of the DSP applications. These facts have been the motivations for realizing this component using the approximate computing approach. This approximate adder has mainly two approaches. Those approaches focus on the error weight and error probability reduction. First approach is based on hybrid adder which has exact and exact LSB are utilized. The error appears in the carry input of the exact most significant bit (MSB) part and the summation in the LSB part.

In second approach, a pure approximate adder is implemented. For these adders reducing error probability as well as reducing delay and power is the key points. They may also be accompanied by an error correction unit which has time, power, and area overheads.

In the RCPA structure, the carry signal propagates in a counter-flow manner from the most significant bit to the least significant bit; hence, the carry input signal has higher significance than the output carry. This method of carry propagation leads to higher stability in the presence of delay variations. The weight of the carry decreases as it propagates. Type of adder improves the energy and delay compared to the normal approximate adder

II. LITERATURE SURVEY

“Performance Analysis of Dadda Multiplier using 5:2 Compressor and its Applications”

Data compression has play major role in compression of the image processing and multimedia. In those applications, reducing area, power and delay are the most important requirements. In this paper two new 5:2 exact compressor are designed to analyze the dadda multiplier based on area, power consumption, and delay.

“Review and Implementation of 4:2 Compressor Based Multiplier Using Verilog”

The scientific literature, which suggests numerous circuits built with approximate 4-2 compressors, has a lot of interest in approximation multipliers. The circuits under investigation are used to create 8x8 and 16x16 multipliers in 28nm CMOS technology.

“Design of Approximate Redundant Binary Multiplier using 5:2 Compressors”

The scientific literature, which suggests numerous circuits built with approximate 4-2 compressors, has a lot of interest in approximation multipliers. The designer who desires to employ an approximation 4-2 compressor faces the difficulty of selecting the suitable topology due to the enormous variety of available alternatives. This paper compares approximate 4-2 compressors already proposed in the literature in this work.

“Design of Approximate Compressors for Multiplication”

Approximate computing is a promising technique for energy-efficient Very Large-Scale Integration (VLSI) system design. It is best suited for error-resilient applications such as signal processing and multimedia. Approximate computing reduces accuracy but still provides significant and faster results with lower power consumption.

III. SYSTEM MODEL

A. Existing Method

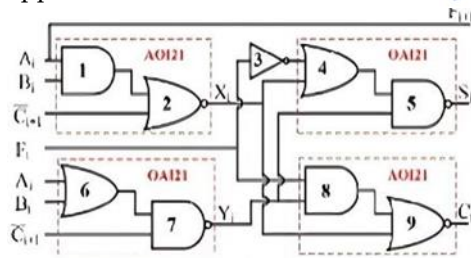
Several approximate 4-2 compressors remove the input and output carry (T_{in} and T_{out}) to reduce circuit complexity. However, this simplification limits the maximum representable value to three, leading to errors when all four inputs are ‘1’. The Yang1 compressor addresses this by introducing a single error, setting Carry (C) = 1 and Sum (S) = 1 in such cases, functioning as a “saturating counter.” In contrast, the Yang2 and Yang3 compressors further simplify the Sum (S) computation but introduce additional errors compared to Yang1. The Lin compressor operates similarly to Yang1 but follows a different error pattern, where $C = 1$ and $S = 0$ when all inputs are ‘1’, causing a discrepancy of two and behaving like a “reflecting 4:2 counter.” The Ha compressor modifies the C output of Yang3, consistently underestimating results and introducing four incorrect entries in the truth table. Meanwhile, dual-quality compressors such as Akbari1 and Akbari2 offer

flexibility by allowing a switch between exact and approximate modes, effectively balancing accuracy and efficiency.

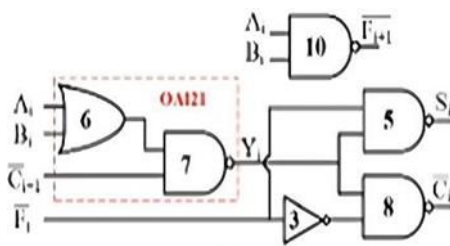
B. Proposed Method

A traditional full adder takes three inputs of equal weight and generates a sum output of the same weight, along with a carry output that has double the weight. The delay caused by carry propagation is crucial since it directly affects the overall speed of multi-bit adders and multipliers. In the worst-case scenario, an n -bit carry propagate adder experiences a delay of $n \times \text{tCP}$, which may introduce setup-related errors.

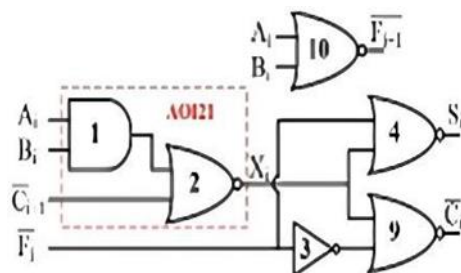
Even slight variations in delay can lead to significant errors in the most significant bits (MSBs) because carry propagation follows a sequential process. By reversing the carry propagation order, the impact of timing variations can be minimized, reducing error magnitude in MSBs. To leverage this idea, an approximate Reverse Carry Propagate Full Adder (RCPFA) has been introduced, aiming to enhance performance and improve reliability in approximate computing applications.



RCPA-1



RCPA-2



RCPA-3

IV. ADVANTAGES

The Approximate Reverse Carry Propagate Adder (ARCPA) offers several advantages, making it highly suitable for energy-efficient DSP applications. One of the primary benefits is its significant reduction in power consumption, as it eliminates or approximates certain carry propagation steps, reducing unnecessary switching activity. This also leads to a faster computation speed, as the critical path delay is minimized compared to conventional adders, making it ideal for real-time processing applications. Additionally, ARCPA designs result in a smaller hardware footprint, requiring fewer logic gates and reducing overall chip area, which is beneficial for low-power embedded systems and mobile devices. While this approach introduces minor errors, it remains well-suited for DSP applications like image and audio processing, where slight inaccuracies do not significantly impact perceived quality. Overall, ARCPA achieves an excellent trade-off between energy efficiency, speed, and hardware complexity, making it an attractive choice for modern approximate computing architectures.

V. APPLICATIONS

The Approximate Reverse Carry Propagate Adder (ARCPA) is widely used in energy-efficient digital signal processing (DSP) applications, where slight computational inaccuracies are acceptable in exchange for reduced power consumption and faster processing. In image processing, ARCPA is beneficial in tasks such as filtering, edge detection, and compression, where minor errors do not significantly degrade visual quality.

Similarly, in audio processing, it is used in noise reduction, speech recognition, and audio compression, as human perception tolerates slight deviations in sound signals. ARCPA is also valuable in machine learning and artificial intelligence, where approximate arithmetic can accelerate training and inference without substantially affecting accuracy. Moreover, it finds applications in wireless communication systems, where it optimizes power efficiency in error-tolerant signal processing tasks. With its advantages in speed and energy efficiency, ARCPA is increasingly being adopted in low-power embedded systems, mobile devices, and Internet of Things (IoT) applications, where power constraints are a critical design factor.

VI. RESULT

An Approximate reverse carry propagate adder is type of adder which generates output carry in counter flow manner from most significant bit to least significant bit. Hence, the carry input signal has higher significance than the output carry compared to this approximate adder, hybrid adder gives the high delay variations in the output.

Comparison of Output Values (CFA vs. RCPFA)

Method	Carry Direction	Sum Calculation	Carry Calculation	Delay	Energy Efficiency	Stability
CFA (Existing)	LSB → MSB	Standard FA Logic	Standard FA Logic	Higher	Higher Power Consumption	Less Stable
RCPFA (Proposed)	MSB → LSB	Uses Forecast Signal (Fi)	Uses Reverse Carry Logic	27% Faster	6% More Energy Efficient	More Stable

VII. CONCLUSION

The Approximate Reverse Carry Propagate Adder designed using pass transistor logic presents a promising solution for energy-efficient DSP applications. By leveraging approximation techniques, the adder achieves significant reductions in power consumption and area, making it highly suitable for applications where exact precision is not critical. Pass transistor logic contributes to further energy efficiency by minimizing transistor count and reducing capacitance, leading to faster switching speeds and lower dynamic power dissipation. Simulation results demonstrate that this design offers a favorable trade-off between accuracy and energy efficiency, maintaining acceptable error rates while significantly enhancing power-performance metrics. Consequently, this approach is ideal for energy-constrained environments such as portable devices, image processing, and real-time signal processing applications. Future work can explore optimization strategies to balance error tolerance and power savings more effectively, paving the way for more advanced low-power computing architectures.

The reverse carry propagation provided higher stability in delay variation. The efficacy of the proposed approximate FAs and the hybrid adders which realized them has been studied in 45-nm technology. The results indicated that utilizing the proposed RCPFAs in the hybrid adders provides, on average, 27%, 6%, and 31% delay, energy, and EDP improvement. As research continues to explore new ARCPAs with improved

accuracy and energy efficiency, their potential for widespread adoption in various DSP applications, including machine learning and artificial intelligence, remains significant.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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