



A Low Power and High Accuracy Approximate Multiplier using 2x1 Multiplexer with Reconfigurable Truncation

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KEYWORDS

Reconfigurable Truncation, Low Power Multiplier, Power Optimization, Area Efficient.

ABSTRACT

Reconfigurable Truncation is a technique that allows for dynamic adjustment of accuracy and power consumption. In multipliers, Reconfigurable Truncation is used to dynamically reduce the number of bits in the output by truncating less significant bits, with the ability to adapt the truncation level based on application requirements, there by optimizing power consumption, area, and processing speed while maintaining acceptable accuracy through techniques like error compensation and control logic. The aim of this project is to design an approximate multiplier with reconfigurable truncation. It evaluates the parameters of Power and Accuracy using VHDL/Verilog Simulation.

1. INTRODUCTION

With the rapid advancement of digital systems, power-efficient and high-performance arithmetic units have become crucial for modern computing applications, particularly in digital signal processing, machine learning, and image processing. However, traditional multipliers require substantial power and area, leading to challenges in designing energy-efficient circuits. Approximate computing has emerged as a promising paradigm to address these challenges by leveraging the

inherent error tolerance in many applications. By allowing a small trade-off in accuracy, approximate multipliers achieve significant reductions in power consumption, delay, and silicon area. Among the various techniques, truncation is widely used to minimize power and complexity by discarding less significant bits. However, fixed truncation schemes lack flexibility, leading to suboptimal accuracy for varying application requirements.

This project explores the design and implementation of a low-power and high-accuracy approximate multiplier using reconfigurable truncation. The proposed design employs transmission gate logic, known for its low-power characteristics and high-speed operation, to achieve efficient multiplication. The reconfigurable truncation technique enables dynamic adjustment of accuracy and power consumption, making the multiplier adaptable to different applications.

By using transmission gate logic, the multiplier benefits from reduced power dissipation, lower leakage currents, and enhanced speed compared to conventional CMOS logic designs. The reconfigurable truncation mechanism enhances versatility, allowing a balanced trade-off between accuracy and energy efficiency. This approach is particularly beneficial for applications such as artificial intelligence, computer vision, and multimedia processing, where power efficiency is crucial. Multipliers are among the most critical arithmetic units in many applications, including DSP, image recognition, and AI. These applications require numerous multiplications, leading to high power consumption, which is a challenge, especially for mobile devices. To mitigate this issue, researchers have explored approximate multipliers, which reduce power and area at the cost of minor accuracy loss. Since many applications are error-tolerant due to human sensory limitations, precise computation is often unnecessary.

Approximate multipliers can be classified into two types. The first approach controls the timing path using dynamic voltage scaling, where reducing voltage increases critical path delay, causing controlled approximation. The second approach modifies the functional behavior of multipliers by redesigning circuits like Wallace Tree and Dadda Tree multipliers. Many existing designs use inaccurate m-n compressors to compress partial products, reducing power consumption and delay.

However, most existing approximate multipliers provide fixed output accuracy and power levels. A dynamically adjustable multiplier is highly beneficial, particularly for AI applications where requirements change over time. To achieve such adaptability, additional hardware cost is inevitable.

II. LITERATURE SURVEY

“Design of power and area efficient approximate multipliers” [1]

Approximate computing improves performance and power efficiency by simplifying design complexity for error-resilient applications. This study introduces an approximate multiplier that modifies partial products based on probability variations. Two 16-bit approximate multipliers achieve 72% and 38% power savings compared to an exact design. They offer higher precision, with mean relative errors as low as 7.6% and 0.02%. In image processing, one multiplier achieves the highest PSNR, proving its superior performance.

“Approximate compressors for error-resilient multiplier design” [2]

Approximate circuit design is crucial for error-resilient image and signal processing. This paper proposes three approximate compressors for partial product reduction (PPR) in a multiplier. It integrates approximation and truncation to enhance efficiency. An image sharpening algorithm demonstrates its practical application. Simulations show significant area and power reductions while maintaining a high SNR (>35 dB).

“High accuracy approximate multiplier with error correction” [3]

A novel approximate multiplier with tunable accuracy modes using an inaccurate 4×4 multiplier is proposed. It achieves 17.98%-34.15% power reduction with a 22.2% maximal absolute relative error. A Gaussian filter for image sharpening improves SNR by 5-22 dB while reducing power and area. An error detection and correction (EDC) circuit enhances accuracy for non-error resilient applications. The design offers minimal area usage compared to other error-correcting multipliers.

“Dual-quality 4:2 compressors for utilizing in dynamic accuracy configurable multipliers” [4]

This paper introduces four 4:2 compressors with switchable exact and approximate modes for dynamic accuracy control. In approximate mode, they achieve higher speed and 68% power savings with a 46% delay reduction in a 32-bit Dadda multiplier. Their effectiveness is validated in image processing

applications, proving their practical benefits. These compressors enable runtime accuracy adjustments for enhanced efficiency.

“Low-power digital signal processing using approximate adders” [5]

This paper explores low-power techniques for portable multimedia devices using approximate computing in DSP. A transistor-level logic reduction simplifies full adders, reducing switched capacitance and critical path delays. Applied to video and image compression, it achieves up to 69% power savings. Error and power models validate efficiency in DSP architectures like DCT and FIR filters. **“Block-based carry speculative approximate adder for Energy – efficient applications” [6]**

This paper presents a low-energy block-based carry speculative approximate adder, which partitions the adder into non-overlapping summation blocks selected from carry propagate and parallel-prefix adders. Carry outputs are speculated using input operands, reducing the carry chain length to at most two blocks. In most cases, only one block is needed, leading to lower average delay. An error detection and recovery mechanism improves accuracy. Compared to state-of-the-art adders, this design achieves an average 50% cost reduction in energy, delay, area, and output quality.

“Approximate multipliers based on new approximate compressors” [7]

Approximate computing enhances speed and power efficiency by relaxing exact computation requirements. This paper proposes novel approximate compressors and an algorithm for designing efficient approximate multipliers. Synthesized using a 40-nm library, these multipliers outperform existing designs in power or speed for a given precision. Their effectiveness is demonstrated in image filtering and adaptive least mean squares filtering applications.

“New metrics for the reliability of approximate and probabilistic adders” [8]

Addition is vital in computing, with inexact adders designed for low-power applications using approximate arithmetic or probabilistic circuits. This paper introduces new evaluation metrics like Error

Distance (ED), Mean Error Distance (MED), and Normalized Error Distance (NED) for accuracy analysis. MED assesses overall accuracy, while NED remains size-invariant, making it a universal metric. The power-NED product ensures a balance between energy efficiency and computational precision for applications in machine learning, DSP, and embedded systems.

“Design-efficient approximate multiplication circuits through partial product perforation” [9]

This paper introduces partial product perforation as a hardware-level approximation technique for energy-efficient multipliers. The method ensures bounded and predictable errors based on input distribution. Extensive evaluations show 50% power savings, 45% area reduction, and 35% critical delay improvement compared to exact designs. The technique is optimized for different error constraints across various architectures. Compared to truncation, voltage overscaling, and logic approximation, it achieves superior power dissipation and error performance. This makes it a promising approach for error-tolerant applications.

“ADIC: Anomaly detection integrated circuit in 65-nm CMOS utilizing approximate computing” [10]

This paper presents ADIC, a low-power anomaly detection IC using a one-class classifier (OCC) neural network. It achieves 42% energy reduction through online learning and approximate computing, with $K = 7$ base learners for dynamic scaling. Fabricated in 65-nm CMOS, it consumes 11.87 pJ/OP for learning and 3.35 pJ/OP for inference. Tested on the NASA bearing dataset, it achieves 18.5× energy efficiency by shutting down 80% of the chip for 99% of its lifetime.

“A reconfigurable FIR filter design using dynamic partial reconfiguration” [11]

This paper presents a novel partially reconfigurable FIR filter design that employs dynamic partial reconfiguration. Our scope is to implement a low-power, area-efficient autonomously reconfigurable digital signal processing architecture that is tailored for the realization of arbitrary response FIR filters. The implementation of design addresses area efficiency and flexibility allowing dynamically inserting and/or removing the partial modules. This design method

shows the configuration time improvement by small configured slice and good area efficiency as compared to the method of conventional FIR filters.

“Separable FIR Filtering in FPGA and GPU Implementations: Energy, Performance, and Accuracy Considerations” [12]

This paper explores dynamic partial reconfiguration (DPR) for 2D FIR filtering, allowing energy, performance, and precision control by adjusting filter coefficients. A high-performance GPU implementation is also presented to compare trade-offs between FPGA and GPU-based designs. Using the Difference of Gaussians (DOG) filter, results show that DPR achieves real-time performance with significantly lower energy consumption, whereas the GPU delivers higher performance but at a much higher energy cost. This study highlights the advantages of FPGA-based DPR for energy-efficient video processing.

III. PROPOSED METHOD

A low-power, high-accuracy approximate multiplier using a 2×1 multiplexer with reconfigurable truncation enhances energy efficiency and hardware simplicity. The 2×1 multiplexer selects partial products, reducing switching activity and computation complexity, leading to lower dynamic power consumption. Like reconfigurable truncation, it adjusts truncated bits dynamically while employing error correction to maintain accuracy. The multiplexer-based architecture improves speed and reduces power usage, making it ideal for AI, DSP, and embedded systems. This design optimizes power, performance, and accuracy trade-offs, making it highly efficient for power-constrained environments. The simplified structure further enhances hardware efficiency with lower complexity than traditional approaches.

1) BLOCK DIAGRAM

- Truncated Partial Product Generation (Stage 1): The inputs undergo truncation using multiple truncation blocks (Trunc₀ to Trunc₃) to reduce complexity before generating partial products.
- Accurate and Approximate Regions (Stage 2): The partial products are divided into two

regions—accurate (left, blue and gray blocks) for precise computation and approximate Region (right, green and black symbols) to optimize power and area efficiency.

- Use of Compressors and Adders (Stage 3): The architecture employs proposed 4-2 compressors, EDC compressors, full adders, and half adders to efficiently sum the partial products while reducing delay and power consumption.

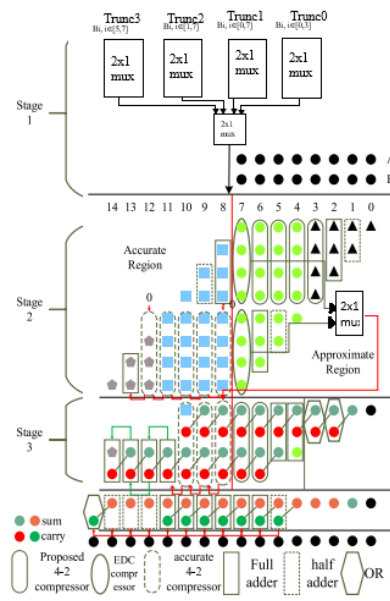
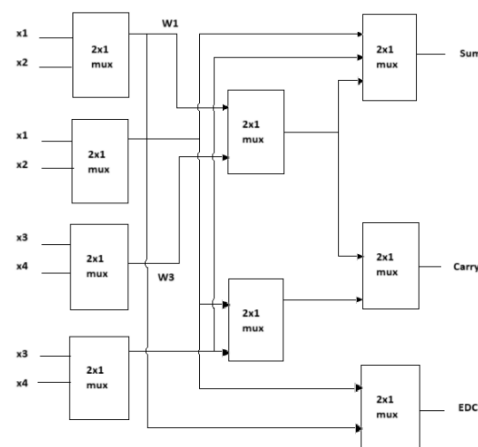


Fig. 3.1. Block Diagram

In the second stage, the 2×1 mux is used to detect the errors in the output.

2) ERROR DETECTION



The architecture presents a low-power and high-accuracy approximate multiplier using 2×1 multiplexers with reconfigurable truncation. It employs multiple multiplexers to selectively compute partial

products, reducing hardware complexity and power consumption. The truncation process dynamically adjusts bit selection to balance accuracy and efficiency. Intermediate signals (W1, W3) manage data flow for efficient computation. Error detection and correction (EDC) help mitigate truncation-induced errors, improving accuracy. The final outputs—Sum, Carry, and EDC—ensure an optimized multiplication result. This design is well-suited for AI, DSP, and embedded applications requiring energy-efficient computation.

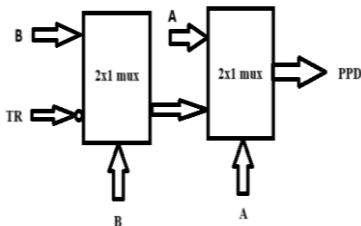
Equation for Error Detection Circuit is given as

$$\text{Error} = W_1 \text{ AND } W_3$$

This enhances the reliability of the system by identifying and potentially correcting errors during compression operations.

3) TRUNCATION

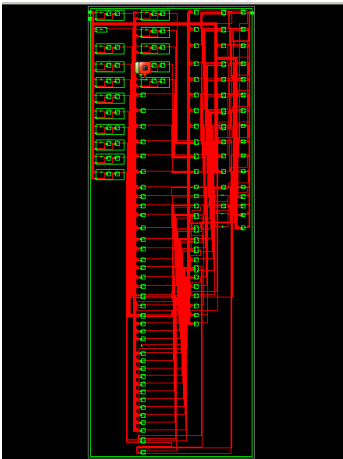
The given diagram represents a 2×1 multiplexer-based approximate multiplication architecture with reconfigurable truncation (TR). This design effectively balances accuracy and energy efficiency in low-power computing applications.



The first 2×1 MUX selects between input B and a truncated signal, controlled by the truncation (TR) input. The output of the first MUX is fed into the second 2×1 MUX, which selects between input A and the previously selected signal. The final output, PPD (Partial Product Data), represents the optimized multiplication result with reduced power and delay.

IV. RESULTS

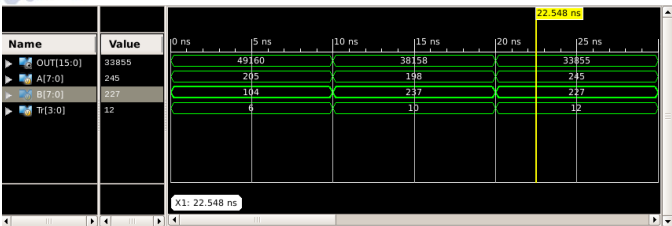
a) RTL Schematic



The layout features a multiplexer-based approximate multiplier with optimized area utilization for power and delay reduction. Red signal paths highlight routing efficiency, though interconnect congestion needs optimization. Enhancements can further improve performance by reducing wire congestion and refining transistor-level design.

b) Simulation Results

The given image represents a timing waveform simulation of a digital circuit, showing signal transitions over time. The X-axis denotes time (in nanoseconds), while the Y-axis represents signal values for different variables such as OUT [15:0], A [7:0], B [7:0], and Tr [3:0].



The cursor at 22.548 ns marks a significant transition point, indicating the circuit's response time. The stable final values confirm the correct functionality of the proposed approximate multiplier using a 2×1 multiplexer with reconfigurable truncation. The simulation helps verify accuracy, delay, and performance of the design for efficient implementation.

c) Evaluation Table

	Area (LUT's)	Delay(ns)	Power(W)
Proposed Method	125	15.870	0.00648
Existing Method	85	20.809	0.00826

The Proposed Method shows a 47.06% increase in area compared to the Existing Method, as it utilizes more LUTs. However, it achieves a 23.74% reduction in delay, improving computational speed, and a 21.55% reduction in power consumption, making it more energy-efficient. While the area overhead is higher, the significant improvements in speed and power efficiency make the proposed design highly suitable for applications requiring low power and high performance.

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Conflict of interest statement

Authors declare that they do not have any conflict of interest.

REFERENCES

- [1] C. S. Wallace, "A suggestion for a fast multiplier," IEEE Trans. Electron. Comput., vol. EC-13, no. 1, pp. 14–17, Feb. 1964.
- [2] T. Yang, T. Ukezono, and T. Sato, "A low-power high-speed accuracy- controllable approximate multiplier design," in Proc. 23rd Asia South Pacific Design Autom. Conf. (ASP-DAC), Jan. 2018, pp. 605–610A.
- [3] Momeni, J. Han, P. Montuschi, and F. Lombardi, "Design and analysis of approximate compressors for multiplication," IEEE Trans. Comput., vol. 64, no. 4, pp. 984–994, Apr. 2015.
- [4] C.-H. Lin and I.-C. Lin, "High accuracy approximate multiplier with error correction," in Proc. IEEE 31st Int. Conf. Comput. Design (ICCD), Oct. 2013, pp. 33–38.
- [5] P. J. Edavoor, S. Raveendran, and A. D. Rahulkar, "Approximate multiplier design using novel dual-stage 4:2 compressors," IEEE Access, vol. 8, pp. 48337–48351, 2020.