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Performance Improvement of BLDC Motor Based on Quasi-Z Source Network

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ABSTRACT

Quasi Z Source network is one of the Z source inverter topologies, Basically it is the combination of Four switch three phase configuration and boost circuit.This paper presents Four switch configuration which has several advantages compared to Six switch three phase configuration, Four switch three phase configuration there by overcoming the limitations of Z source network. A novel Four switch three phase BLDC motor control scheme based on Quasi Z source network improves the utility ratio of DC voltage and extends the range of speed. During the operation of the motor, shoot through states are inserted then the input voltage of the inverter increases and performance of the motor is markedly improved. The proposed method uses Level shifted PWM technique and reduces the distortion in phase currents there by improving the speed of the motor. The controlling method for existing model and proposed model is studied in detail and constructed in Matlab/ simulink environment.

Keywords: *Brushless DC Motor, Quasi Z Source Network, Shoot Through, Level Shifted PWM, Matlab/ Simulink.*

I. INTRODUCTION

Brushless DC motor is widely used in various fields, because of its high power density, large output torque and quick dynamic response, etc. Four-switch three-phase brushless DC motor is developed based on the driving circuit that is composed of conventional six-switch inverter. It has the advantages of low-driven cost and less switching loss. Therefore, it is of great significance to research on performance enhancements of four-switch three-phase brushless DC motor.

The four-switch three-phase (FSTP) BLDC motor has the characteristics of lower cost and switching loss, the research on control method and its performance becomes a hot-spot issue. The direct current control has been proposed in paper [1] by detecting and controlling the currents of different active phases independently, and the C phase back-EMF is compensated, the distortion of currents is minimized. The effective-vector current control has been presented in [2]-[3], the C phase current is controlled to be zero nearly by inserting adjusting vectors when the active phases are A and B. The control method has the merits of constant switching frequency, simple construction, etc. Combining FSTP inverter with boost circuit, a novel five-switch three-phase topology has been presented in paper [4].

In the paper, a new topology of FSTP BLDC motor drive system is proposed. The function of boosting voltage is added by employing a quasi Z-source

network. In two modes, the bus voltage of inverter increase until the rated value when the upper and lower devices of one bridge arm are gated simultaneously. Simulations were constructed in MATLAB/Simulink circumstance. The experiments showed that the utilization of DC-link voltage could be improved, and the range of speed could be extended.

II. OPERATING PRINCIPLE OF FSTP BRUSHLESS DC MOTOR

The conventional topology of FSTP brushless DC motor is shown in Fig.1, and the DC bus voltage is U_{dc}. The phase current of stator windings are driven

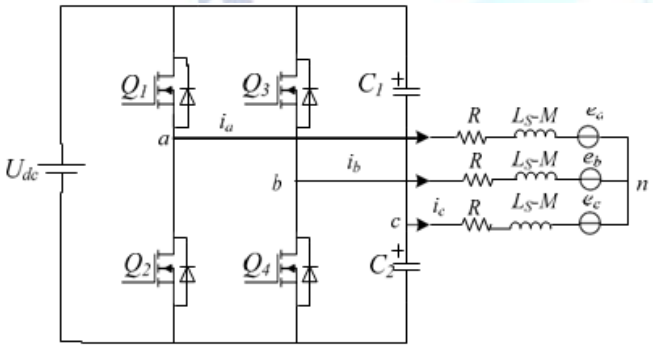

Fig 1: Topology of FSTP configuration

On the other hand, due to C phase of motor is connected to the mid of two capacitors in series, three phase currents affected by C phase back-EMF are unexpected and distorted in mode II and V.

According to Fig.2, it is the circuit topology of QZFSTP brushless DC motor driver. The partial circuit of quasi Z-source converter is added before the input of FSTP inverter. Moreover, the power switch Q_5 is applied between the bridge arm of phase A and phase B. The current control scheme based voltage vector is adopted, and the working time of voltage vector is determined through the speed and current double closed loop.

The Quasi Z-source converter is an improved configuration based on Z-source network and is composed of two equivalent inductors and two equivalent capacitors. Theoretically, the output can be boosted to any DC voltage when switch shoot through duty ratio is smaller than 50%.

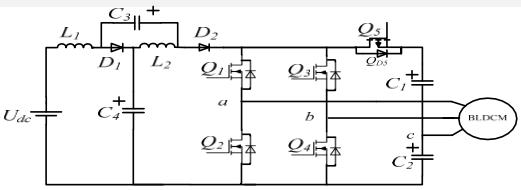

Fig 2: Circuit topology of QZFSTP brushless DC motor drive

The average output voltage is

$$V_o = \frac{1}{1-2D} V_{in} \qquad (1)$$

As shown in (1), D is the short through duty cycle. The output voltage is greater than the input one as long as D is less than 0.5

TABLE I
STATUS OF DEVICES IN SIX MODES OF FSTP MOTOR

Mode	Hall sensor	Active phase	Silent phases	Conducting devices
I	001	C/B	A	Q_1
II	101	A/B	C	Q_1 Q_4
III	100	A/C	B	Q_4
IV	110	B/C	A	Q_3
V	010	B/A	C	Q_3 Q_2
VI	011	C/A	B	Q_2

In total 13 voltage vectors are used in this scheme *V(10000), V(00100), V(10001),V(10011), V(00011), V(00101), V(01101) , V(01001),V(01000), V(11000), V(00010), V(00110) and V(00000).*

In this paper, the current control strategy based on voltage vector is applied for the QZFSTP BLDC motor. Six modes are divided into three cases. The first one conventional bipolar modulation is used in mode III, IV. The second one is that the adjusting voltage vector is added to modify the C phase current in mode II, V. The last one is that the shoot-through state of switches is added in order to boosting the DC voltage in mode I, VI. Then, the control method of QZFSTP motor in each mode is analyzed in details.

A. MODE III and IV

Fig.3 shows the switching sequence of five power switches and the time of voltage vector in mode III, IV, in which the operation time of master vector is T_1 and the zero vector is T_0. The *V*(00000) has two functions: the first one is adjusting the phase current, the other one is reducing switching loss (especially in mode II, V). The current and speed closed-loop control is adopted in the system, which contain PI controller. The value of T_1 is derived from PI regulator of the current loop output. Besides, T_s minus T_1 is T_0, where T_s is the time period.

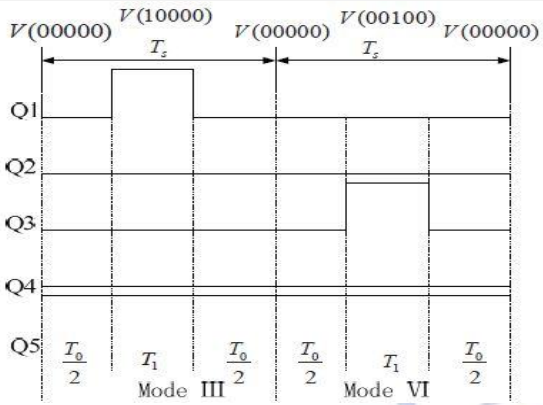

Fig3: switching sequence of five switches in modeIII and IV

B. Mode II and V

Ideally, the A and B phases are active and the C phase is silent in mode II, V. However, the C phase current cannot keep zero in the actual system. It is due to that the C phase is connected to the midpoint of capacitors in series and the C phase back- EMF exists. If the upper and lower devices of one phase arm are gated by the same control signal as in mode III, IV, the distortion of phase current will be caused and the control strategy will be ineffective.

The solution for above problems is that two switches of one bridge should be controlled independently according to the C phase current. Taking mode II as an example, the feasibility of this method is analysed theoretically.The phase voltage equations during switches working can be described as follows

$$U_{ag} = SU_{dc} = Ri_a + (L_s - M)\frac{dia}{dt} + e_a + U_{ng}$$

$$U_{bg} = (1\text{-}S)\,U_{dc} = Ri_b + (L_s - M)\frac{dib}{dt} + e_b + U_{ng} \quad (2)$$

$$U_{cg} = Ri_c + (L_s - M)\frac{dic}{dt} + e_c + U_{ng}$$

Where U_{xg} represents voltage between x phase and ground, $e=e_a+e_b+e_c$, and S is the switching signals of Q_1 and Q_4.And S=0 means switch off and S=1 means switch on.

The voltage between n point and ground is given (2) by

$$U_{ng} = \frac{1}{3}[U_{dc} + (U_{cg} - e)] \quad (3)$$

From (3) the value of U_{ng} is not influenced by S,but it has relationship with $U_{cg} - e$.

$$U_{cg} - e = \frac{1}{6}U_{dc} \Rightarrow U_{ng} = \frac{1}{2}U_{dc} \Rightarrow i_c = 0$$

$$U_{cg} - e \neq \frac{1}{6}U_{dc} \Rightarrow U_{ng} \neq \frac{1}{2}U_{dc} \Rightarrow i_c \neq 0 \quad (4)$$

Equation (4) illustrates the factor leading to the distortion of phase C current.Therefore Q_1 and Q_4 should be controlled independently.Then there will be some changes in (2) and is given as

$$U_{ag} = S_1 U_{dc} = Ri_a + (L_s - M)\frac{dia}{dt} + e_a + U_{ng}$$

$$U_{bg} = (1\text{-}S_4)\,U_{dc} = Ri_b + (L_s - M)\frac{dib}{dt} + e_b + U_{ng}$$

$$U_{cg} = Ri_c + (L_s - M)\frac{dic}{dt} + e_c + U_{ng}$$

Where S_1 is the switching signal of Q_1 and S_4 is Q_4.similarly the following equation can be obtained.

$$U_{ng} = \frac{1}{3}[U_{dc} + (U_{cg} - e)] + (S_1 - S_4)U_{dc}$$

$$U_{cg} - e = \frac{1}{6}U_{dc} \Rightarrow U_{ng} = \frac{1}{2}U_{dc} \Rightarrow i_c = 0$$

$S_1 = S_4$

$$U_{cg} - e > \frac{1}{6}U_{dc} (i_c<0) \Rightarrow U_{ng} \downarrow \Rightarrow i_c \uparrow$$

$S_1 = 0$ $S_4 = 1$

$$U_{cg} - e < \frac{1}{6}U_{dc} (i_c<0) \Rightarrow U_{ng} \uparrow \Rightarrow i_c \downarrow$$

$S_1 = 1$ $S_4 = 0$

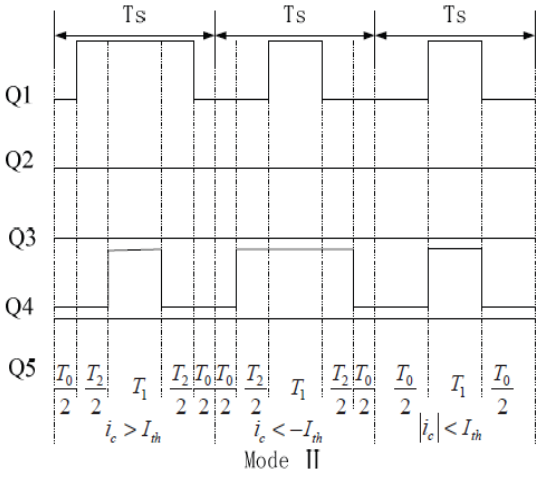

Fig 4: switching sequence of five switches in mode II

For the above formulas i_c can be adjusted close to zero by choosing appropriate states of Q_1 and Q_4.So there are four voltage vectors working in mode II.In fact C phase current cannot be made zero and I_{th} is the small value which is close to zero.So by comparing actual C phase current with I_{th} the value can be adjusted.The same control method can be applied to mode V.

C Mode I and VI

As shown in Fig. 5(a), it is equivalent circuit when the upper and lower devices of phase leg are gated simultaneously. At the moment, the power U_{dc} and capacitor C_3 recharge inductance L_1, and L_1 stores energy. Also, the capacitor C_4 recharges inductance L_2, and L_2 stores energy. The brushless

DC motor is fed by the power of capacitor C_2. The reverse bias voltage across diode D_1 blocks itself from working. The reason why Q_5 is switched off is preventing the capacitor C_1 and C_2 from being short circuited.

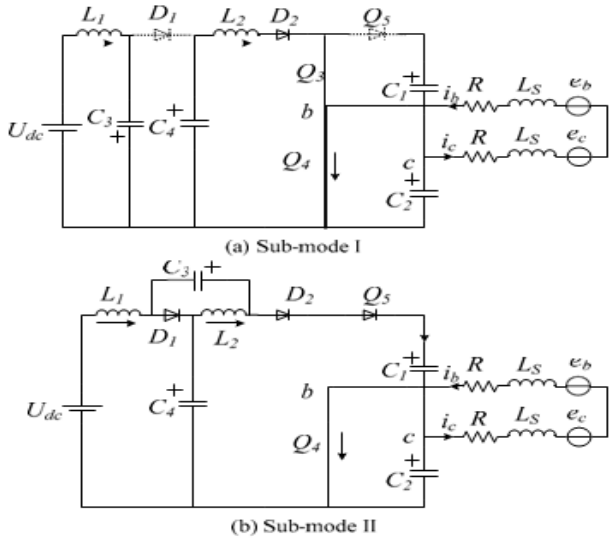

Fig 5: Boosting voltage in mode I and VI

The equivalent circuit when the switch Q_4 is on is shown in Fig. 5 (b). In this case, the inductances release energy. The power U_{dc} and inductance L_1 recharge capacitor C_4, also the inductance L_2 recharges capacitor C_3. Hence, the voltage of inverter side rises to the sum of U_{dc}, C_3 and L_2. For the sake of reducing switching power loss, the switch Q_5 should keep off. Therefore, there are three voltage vectors participating in work, and they are $V(00000)$, $V(00001)$ and $V(00110)$ in mode I. Same explanations can be found in mode VI

III. PROPOSED METHOD

In the proposed method we implemented Level shifted PWM instead of SPWM method.

A Phase opposite Disposition POD

Phase Opposite Disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference. The modulating signal of each phase is displaced from each other by 120°. All the carrier signals have same frequency FC and amplitude AC while the modulating signal has a frequency of fm and amplitude of Am. The fc should be in integer the multiples of fm with three-times. This is required for all the modulating signal of all the three phases see the same carriers, as they are 120° apart.

The carrier waves and the modulating signals are compared and the output of the comparator defines the output in the positive half cycle the comparator output will have the value high, if the amplitude of the modulating signal is greater than that of the carrier wave and zero otherwise. Similarly for the negative half cycle, if the modulating signal is lower than the carrier wave the output of the comparator is high and zero otherwise.

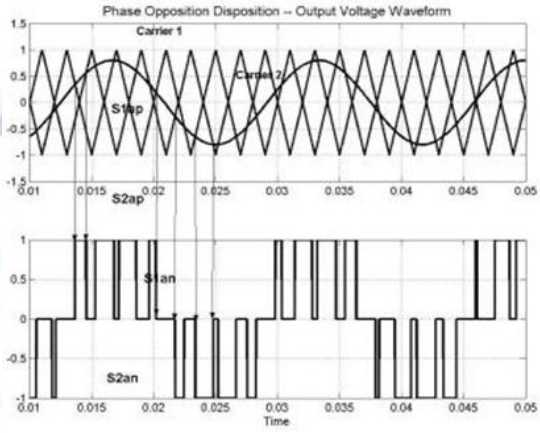

Fig 6:Simulation of carrier-based PWM scheme using POD.(a)Modulation signal and phase carrier waveforms (b)Phase "R" output voltage.

IV. SIMULATION RESULTS

The Quasi Z source network configuration has following parameters C_1=C_2=4700μF and L_1=L_2=45mH.The nominal parameters of the brushless DC motor are as follows:24V(rated voltage),31W (rated power),2000r/min(rated speed), 0.5Ω (stator resistance),0.5mH(stator inductance).

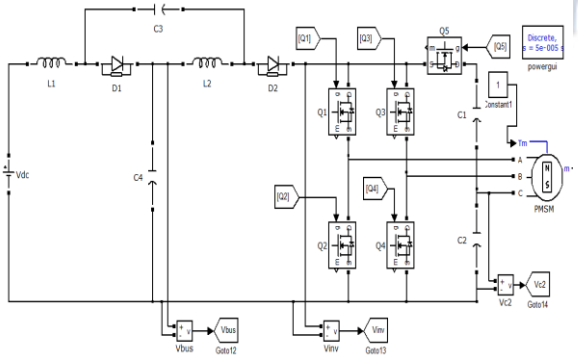

Fig 7: Quasi Z source network configuration

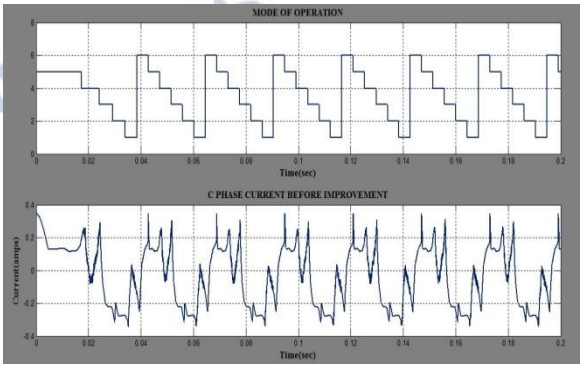

Fig 8: C phase current before improvement

In the fig 8 as shown C phase current is severely distorted when the shoot through states are not inserted. At the time 0.02 sec the distortion of current happens.By the insertion of shoot through states the C phase current is greatly improved.

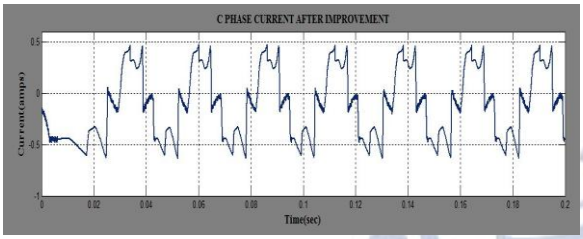

Fig 9:C phase current after improvement

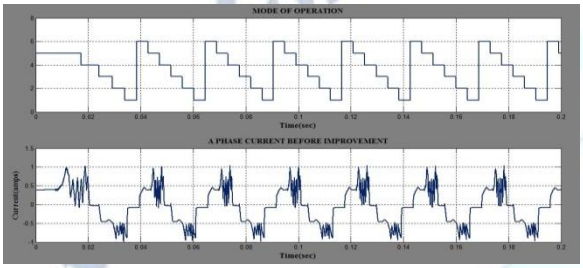

Fig 10 :A phase current before improvement

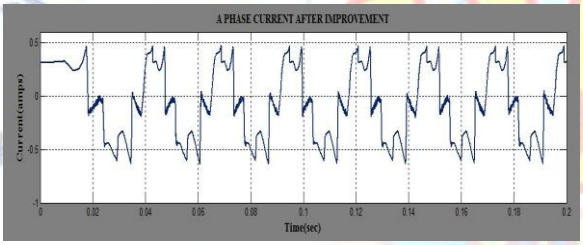

Fig 11:A phase current after improvement

In the fig 10 A phase current is distorted , by the insertion of shoot through states A phase current is improved which is shown in fig 11.The asymmetrical voltages are adjusted by detecting the other phase currents and distortion in A phase currents is clearly improved by boosting the voltage on the input side of the inverter.

According to the fig 12, by the insertion of shoot through states the DC bus voltage of the inverter is 28.5V and the input voltage of the inverter is boosted to 72V.

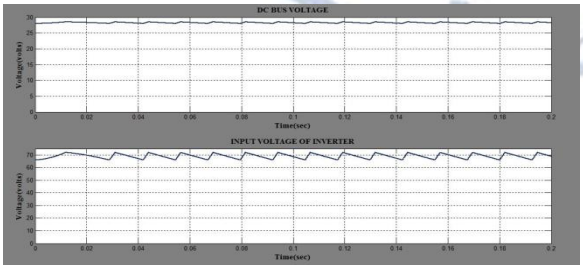

Fig 12: DC bus voltage

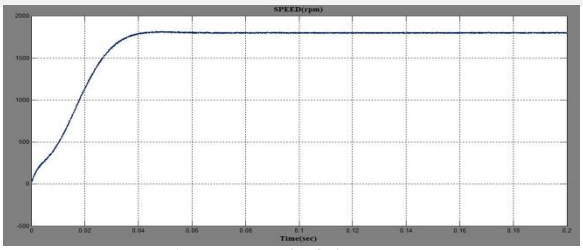

Fig 13:Speed of the motor

The motor achieves speed of 1800 rpm from 0.04 sec, there by dynamic response of the motor is achieved quickly.

V. PROPOSED METHOD

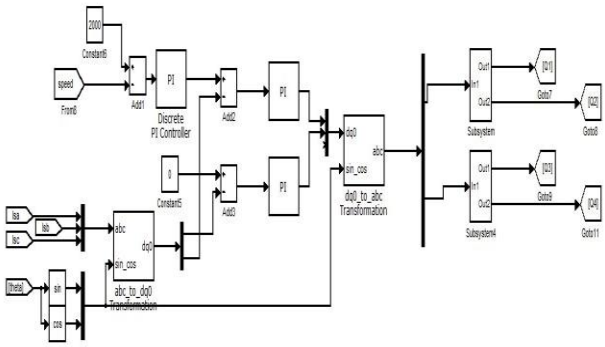

Fig 14: Level shifted PWM

The proposed method uses Level shifted PWM which clearly reduces the distortion in phase currents and speed of the motor is extended to 2000 rpm

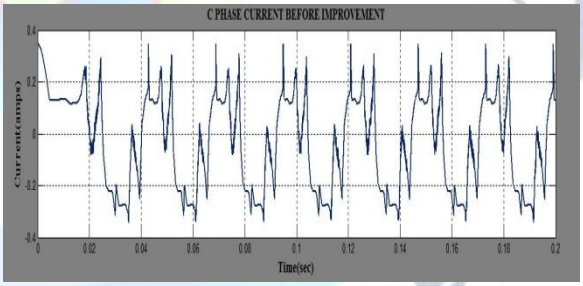

Fig 15:C phase current before improvement

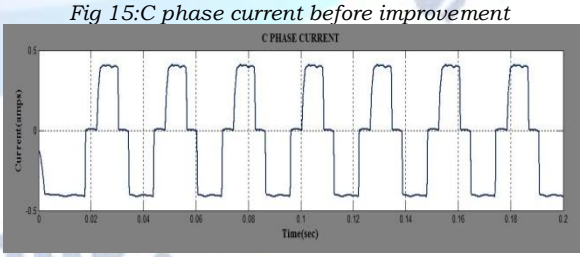

Fig 16: C phase current after improvement

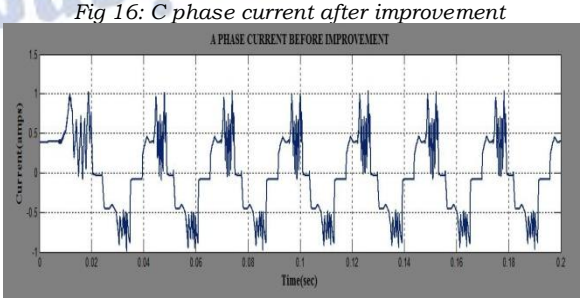

Fig 17: A phase current before improvement

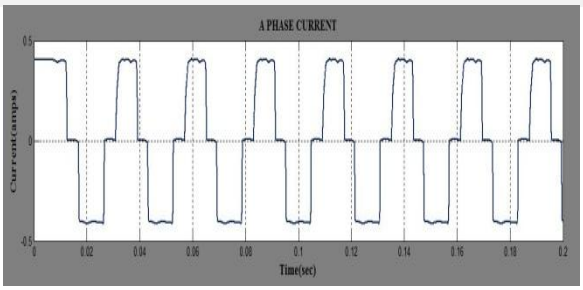

Fig 18 : A phase current after improvement

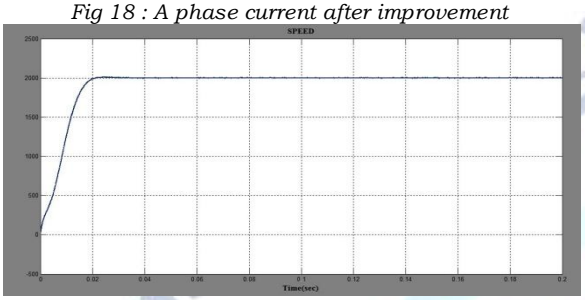

Fig 19: Speed of the motor

VI. FFT ANALYSIS

A Fast Fourier transform algorithm computes the discrete fourier transform of a sequence or its inverse.Fourier analysis converts a signal from its original domain to a representation in frequency domain or vice versa.

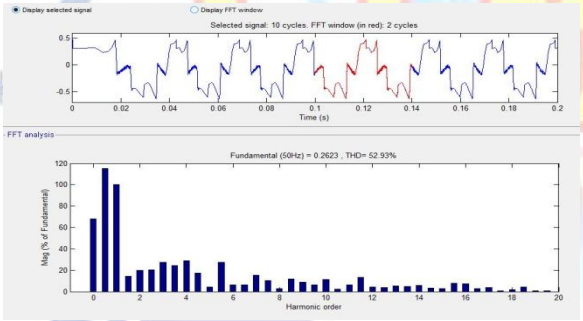

Fig 20: FFT analysis for A phase current (SPWM)

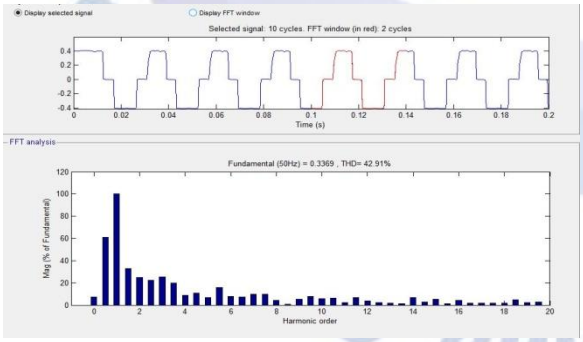

Fig 21: FFT analysis for A phase current (Level shifted PWM)

In the figure 20 FFT analysis is done for A phase current which uses Sinusoidal PWM, Here we considered 2 cycles of A phase current for the analysis with the start time of 0.1 sec, fundamental frequency as 50HZ.In the figure 6.15 the highlighted red portion shows the selected cycle which gives the total harmonic distortion as 52.93%.

In the same way figure 21 is the FFT analysis for A phase current which uses Level shifted PWM, Here the same parameters of 2 cycles with start time of 0.1 sec , is considered with fundamental frequency as 50HZ, the total harmonic distortion is reduced to 42.91%.

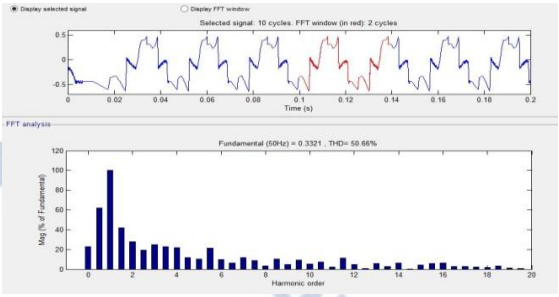

Fig 22: FFT analysis for C phase current (SPWM)

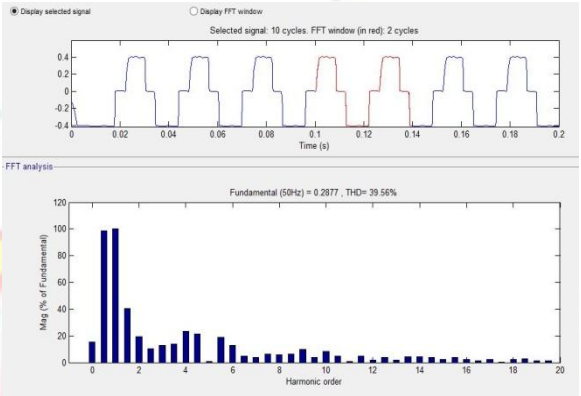

Fig 23: FFT analysis for C phase current (Level shifted PWM)

As shown in the figure 22 FFT analysis is done for C phase current with start time of 0.1sec and fundamental frequency of 50HZ which gives total harmonic distortion as 50.66%, In the similar way with the same parameters FFT analysis is done for C phase current which uses Level shifted PWM and the total harmonic distortion is reduced to 39.56% as shown in the figure 23.

VII. CONCLUSION

A novel four-switch three-phase brushless dc motor control scheme based on quasi Z-source network is presented in the paper, which combines FSTP BLDC motor and quasi Z-source network,Along with that here we presented the SPWM method and Level shifted PWM.The experimental facilities are constructed and its results suggest:

1. In mode II and IV, the distortion of phase current caused by C phase back-EMF is minimized by gating two switches independently.
2. The input voltage of FSTP inverter is boosted to enlarge the range of speed and enhance the ability with load when quasi Z-source converter works.
3.The validity of PWM works effectively on this converter.

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