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Design and Implementation of 32-Bit ALU using QCA Technique

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ABSTRACT

The conventional transistor based CMOS technology has followed Moore's law, doubling transistors every eighteen months. QCA stands for Quantum dot cellular Automata. QCA is an advanced nanotechnology that attempts to create general computational at the nano scale by controlling the position of single electrons. QCA encodes binary information in the charge configuration with in a cell. No current flows out of the cell so that low power dissipation is possible. In ALU adder plays a vital role. This paper describes the design and implementation of 2-bit ALU based on Quantum dot cellular automata using Xilinx 14.7 synthesis and simulation tool. In this survey a binary adder is taken for analysis and a new adder is designed based upon QCA technology. This modified novel bit adder is implemented into ALU structure. The aim of the proposed technique is that to reducing no. of majority gates used in the design.

Keywords: *QCA-Quantum dot cellular automata, Xilinx ISE, CMOS*

I. INTRODUCTION

A) CMOS Technology

There has been extensive research in recent years at nano scale to supersede conventional CMOS technology. Microprocessor manufacturing processes was governed by Moore's law, and consequently microprocessor performance till now. Today many integrated circuits are manufactured at 0.25-0.33 micron processes. But recent studies indicate that as early as 2010, the physical limits of transistor sizing may be reached [2]. However the performance of various circuits in current CMOS-based architectures is close to reaching the limit.

If the feature size of transistors is further reduced to a nanometer, it will produce quantum effects such as tunneling. Further, during device scaling process due to the effects of wire resistance and capacitance, the interconnections never scale automatically. Addition is an essential operation many Digital, Analog, or Control system [9]-[12]. Fast and accurate operation of all digital system depends on the performance of adders .The main function of adder is to speed up the addition of partial products generated during multiplication operation. Hence improving the speed by reduction in area is the main area of research in VLSI system design.

B) QCA Technology

As an alternative to CMOS-VLSI, an approach called the quantum cellular automata (QCA) is developed in 1993[1] to computing with quantum dots. Unlike conventional computers in which information is transferred from one place to another by electrical current, QCA transfers information by means of propagating a polarization state from one cell to another cell [7].The charge distribution in each cell is aligned along one of two perpendicular axes, so that the binary information can be encoded by using the state of the cell.

Tree adder is an alternate to conventional adder, because by using tree structure carries are generated in parallel and fast computation is obtained at the expense of increased area so power usage is also increased. The main advantage of this design is that the carry tree reduces the number of logic levels(N) by generating the carries in parallel. The parallel prefix tree adders are more favorable in terms of speed due to the complexity O(log2N) delay through the carry path compared to that of other adders[6].

II. Background

A quantum-dot cellular automaton (QCA) is based on field coupled computing. States of a cell change due to mutual interactions of either electrostatic or magnetic fields. QCA Cell is the fundamental component of QCA Logic. Each QCA cell is made of four quantum dots in which two mobile electrons can be trapped which can tunnel between the dots. Due to the repulsion between the electrons, two electrons always take up the diagonal positions. Binary levels are represented by the positions of the electrons inside the cell unlike the voltage or current levels as in the CMOS. Fig.1 show the structures of quantum cell with two different polarizations (electrons are shown with black filled circular dots).

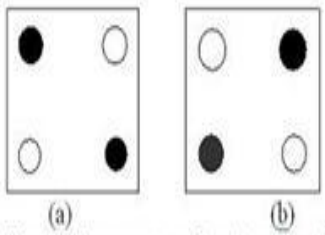


Fig.1. QCA cells with four quantum dots (a) cell with polarization p= -1(Logic '0') (b) cell with polarization p = 1 (Logic '1')

Majority gate and Inverter are the two basic logic devices of QCA. Fig.2 shows the structure of the majority gate with 3 inputs, driver cell and output cell. Computation starts by driving the driver cell to the lowest energy state. Input cell changes its state by the signal which arrives towards the driver cell. Driver cell always gets the binary value of majority of input signals since it is where the repulsion for the mobile electrons in driver cell is at minimum and output follows the state of driver cell.

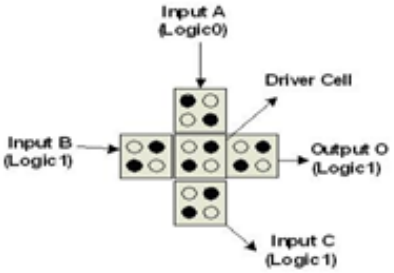


Fig.2 Majority Gate

The logic function for the majority gate is given by M(a,b,c) = ab+bc+ca with a, b, c as boolean variables. In this way two input AND, OR gates can be designed by keeping the third variable as either 0 or 1 respectively. Inverter is the other basic logic device of QCA. If cells are placed diagonally to each other then they will have opposite polarizations. QCA Inverter is designed by this characteristic, such as shown in Fig.3

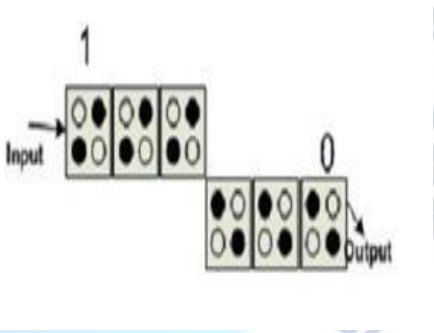


Fig.3. QCA Inverter

III. Conventional QCA Adders

1-Bit ALU Architecture:

The Arithmetic logic unit performs the basic arithmetic and logical operation. The ALU consists of arithmetic extender, logical extender and a full adder which is shown in fig 4. Three control signals will decides the operation of the ALU. M is the mode control variable which select between arithmetic and logical operations. S1 and S0 are selection line used in combination with M to select between the eight arithmetic and logical operation the ALU supports. Detail about Arithmetic and Logical extender is explained in [8].

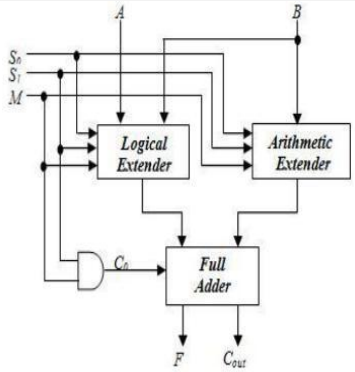


Fig .4: Architecture of ALU

Three control signals determine the operation of the ALU. M is the mode control variable used to select between arithmetic and logical operations. S1 and S0 are used in combination with M to select between the eight arithmetic and logical operation the ALU supports.

A) Arithmetic Extender:

The Arithmetic extender modifies the second operand and passes it to the Full adder to the arithmetic as shown in Table I and Table II.

TABLE I. FUNCTION TABLE OF ARITHMETIC EXTENDER

M	S_1	S_0	Function name	Function	X	Y	C_0
1	0	0	Decrement	A-1	A	all 1's	0
1	0	1	Add	A+1	A	B	0
1	1	0	Subtract	A+B'+1	A	B'	1
1	1	1	Increment	A+1	A	all 0's	1

TABLE II. TRUTH TABLE OF ARITHMETIC EXTENDER

M	S_1	S_0	B	Y
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	0	0
1	1	1	0	0
1	1	1	1	0

According to truth table we write Boolean

The proposed n bit QCA adder consists of 4n+ 1 number of majority gates and n+2 inverters. It results in reduced hardware compared to the existing [5] structure and retains the simple clocking scheme.

equation of arithmetic extender shown in equation (1) and design logic circuit of arithmetic extender shown in fig. 5.

$$Y = M\bar{S}_1 B + M\bar{S}_0 \bar{B} \quad (1)$$

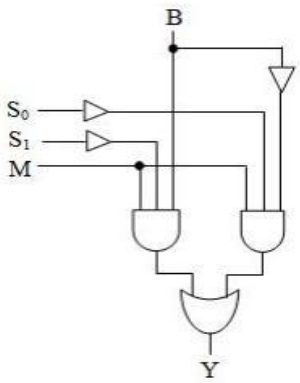


Fig 5: Logic Circuit of Arithmetic Extender

B.Logical Extender:

The logic operations are performed in the logic extender as evident from Table III and Table IV. The FAs are used simply as connection for the outputs. According to truth table we write Boolean equation of logical extender shown in equation (2) and design logic circuit of logical extender shown in fig. 6.

TABLE III. FUNCTION TABLE OF LOGICAL EXTENDER

M	S_1	S_0	Function Name	Function	X	Y	C_0
0	0	0	Complement	A'	A'	0	0
0	0	1	AND	A and B	A&B	0	0
0	1	0	Identity	A	A	0	0
0	1	1	OR	A or B	A|B	0	0

TABLE IV. FUNCTION TABLE OF LOGICAL EXTENDER

M	S_1	S_0	X
0	0	0	A'
0	0	1	A & B
0	1	0	A
0	1	1	A | B
1	X	X	A

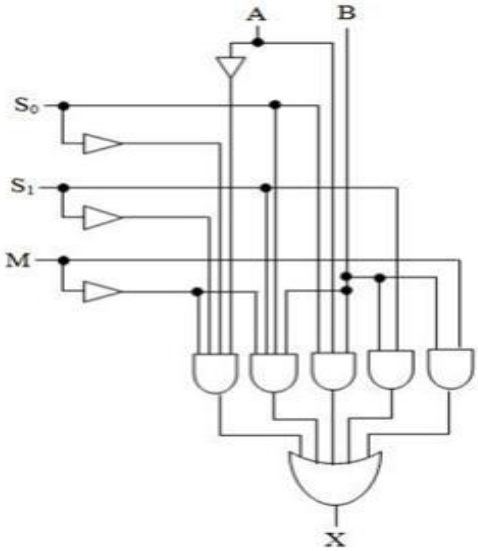


Fig 6: Logic Circuit of Logical Extender

IV. Proposed QCA Adder

In this section, we propose a two new QCA addition algorithm and the corresponding two-bit QCA adder structure that reduces the number of the majority gates and inverters required for existing designs [5] and eliminate above mentioned drawback also.

i) Modified Bit adder1: To introduce proposed Modified novel bitadder 1 – n bit architecture first it is designed a 2bit basic module based on proposed algorithm. let us consider 2 operands such as A=a1aO and B=b1bO and we designed proposed 2bit module as shown in fig 7.1(a).For each bit the carry is generated by using one majority gate. Sum is calculated by cascading of 3 MG's. Given three inputs a, b, and c, the MG performs the logic function reported in (3). Provided that all input cells are associated to the same clock signal c1kx (with x ranging from 0 to 3).

M (a,b,c)=a.b+b.c+c.a (3)

To create an n-bit adder, let consider two n bit addends A = an-I, ... , aO and B = bn- I, ... , bOand for i = n - 1, ... , 0 and we arrange n proposed one-bit adders vertically in a column which is shown in fig7.1(b) and
7.1(c)respectively

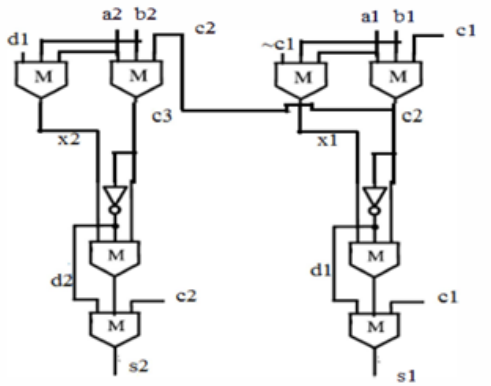


Fig 7.1(a): Modified novel bit adder 1: 2 bit basic Module

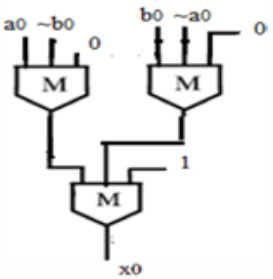


Fig 7.1(b): Modified novel bit adder 1-Calculation of xO

This proposed architecture can be implemented by using equation (4) and (5)

Ci+1= M (ai,bi,ci) (4)

Si=M (M (M (ai, bi, di-1), M (ai,bi,ci), di), di, Ci) (5)

Where di=~ci+1

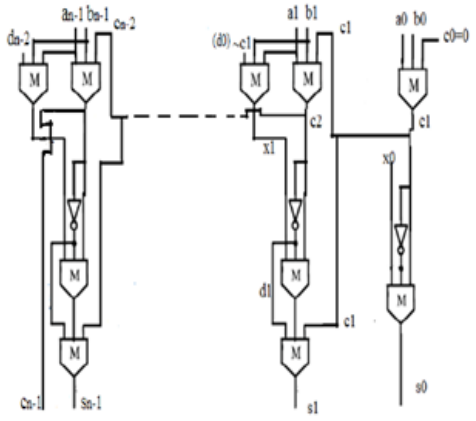


Fig 7.1(c): Modified novel bit adder I: n bit basic Module

ii) Modified Novel Bit adder 2: Here we now introduce a new Modified novel bit adder 2- n bit adder architecture which reduces hardware complexity compared to existing[5] and Modified novel bit adder 1 structure. The basic 2bit module for Modified novel bit adder 2 is shown in fig 7.2(a).Here the carry is calculated in same way as in proposed 1 structure and sum block is modified which requires two majority gates only.

This proposed architecture can be implemented by using equation (6) and (7)

Ci+1= M (ai,bi,ci)..... (6)

Si=M(M (ai, bi, di-1), di, Ci) ..... (7)

Where di=~ci+1

To create an n-bit adder, let consider two nbit addends A = an- I, ... , aO and B = bn- I, ... , bOand for i = n - 1, ... , 0 and we arrange n proposed one-bit adders vertically in a column which is shown in fig 7.2(b).

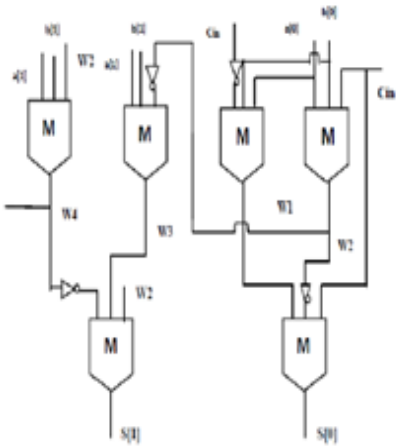


Fig 7.2(a): Modified novel bitadder 2: 2bit basic Module

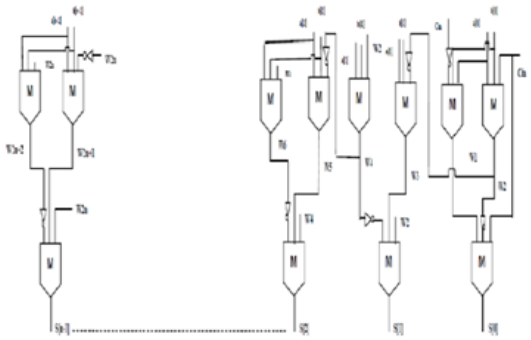
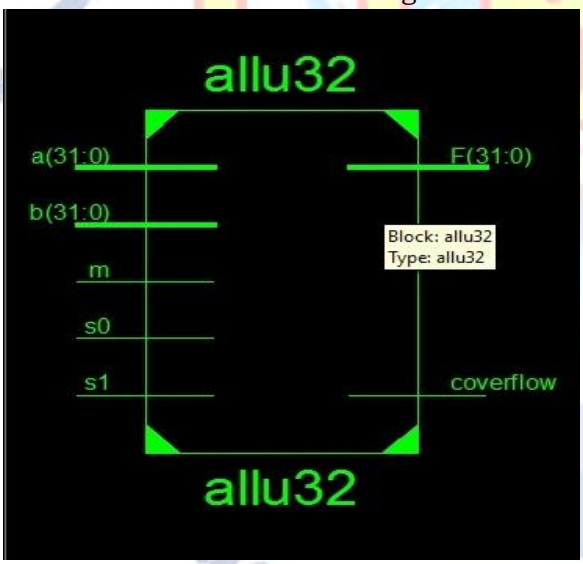


Fig 7.2(b): Modified novel bit adder 2: n bit adder

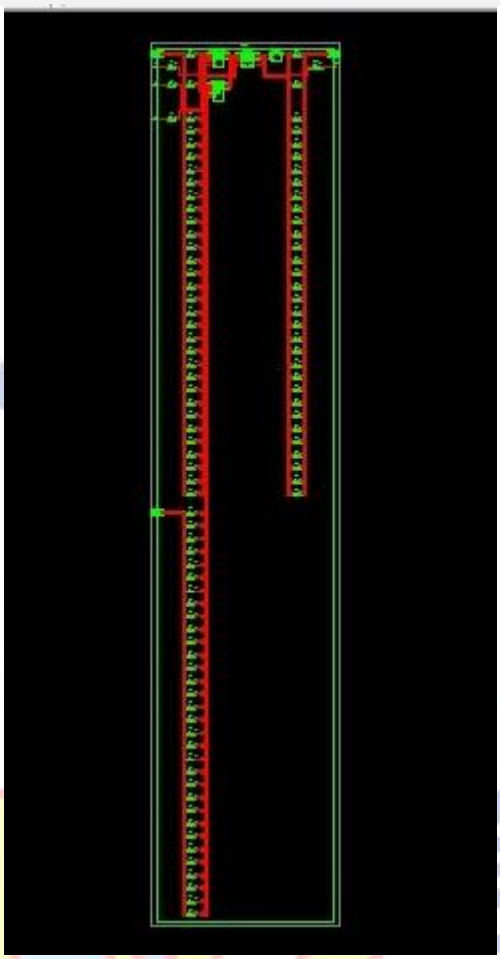
The proposed n bit QCA adder consists of 3n number of majority gates and n inverters. It results in reduced hardware compared to the existing [5] structure and proretains the simple clocking scheme.

V. Simulation Results

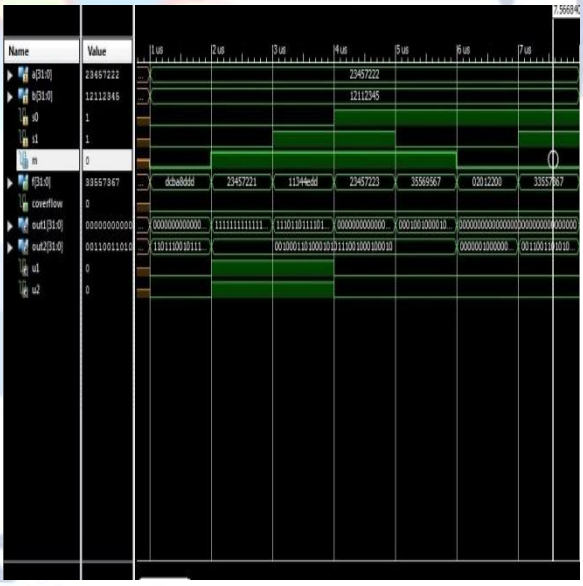
Simulation IS performed by using Xilinx 14.7i simulation tool and the operation is checked for all the input combinations. The synthesis and simulations are as shown below figures.



32 bit QCA ALU Schematic



32 bit QCA ALU Technological Schematic



32 bit QCA ALU Simulation Result

VI. Conclusion

The proposed 32-bit high speed QCA ALU is simulated through integrated Xilinx simulator and the code is functionally verified to be correct. The proposed 32-bit high speed QCA ALU architecture requires Majority Gate than the existing method.

Hence, the active area is decrease and consequently consumes lesser power than the existing method. The QCA technology is particularly suitable for high throughput and deeply pipelined architectures Applications such as audio and video stream processing benefit much with QCA architectures. Quantum dot Cellular Automata (QCA) attempts to create general computational at the nano-scale by controlling the position of single electrons. It overcomes the limitations of CMOS technology. With the increment of no of bits, the speed of ALU increases, i.e., 32bit is more faster than 16 bit ALU design using QCA technology.

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