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Reduction in Harmonics using 7-Level Inverter with Reduced Number of Switches

N.Karthika[1] | G.Purushothaman[2] | S.Priyanka[3] | M.Rajaganapathi[4]

[1,2,3,4] Department of EEE, M.A.M.S.E, Trichy, India.

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ABSTRACT

This paper presents a topology with a reduced number of switches, which is used to reduce the total harmonic distortion (THD%) using MCPWM technique, MCPWM with trapezoidal reference wave and also SHE technique such as PSO technique and Newton-Raphson (NR) technique. SHE technique is used to eliminate a particular harmonic in a multilevel inverter (MLI);the MCPWM and Trapezoidal reference wave techniques are also used to reduce the harmonics present in the MLI with a triangular wave which acts as a carrier wave .This topology is also used to improve the multilevel performance .The performance evaluation of the proposed PWM, Trapezoidal reference wave and SHE techniques for a MLI is done by using MATLAB/Simulink and THD is analysed. It is observed that PSO technique produces a better fundamental voltage output and less THD.

KEYWORDS: *Multicarrier Pulse Width Modulation (MCPWM), Selective Harmonic Elimination (SHE), Particle Swarm Optimization (PSO), Newton-Raphson (NR) and Total Harmonic Distortion (THD).*

I. INTRODUCTION

The term "multilevel inverter" was rooted years ago. Mul-tilevel inverters offer various applications in voltage rang-ing from medium to high such as in renewable sources, industrial drives, laminators, blowers, fans, and conveyors. Small voltage step results in making the multilevel inverters withstand better voltage, fewer harmonics, high electro-magnetic compatibility, reduced switching loss, and better power quality [1].

Cascaded multilevel inverters were developed in the initial stage. Later, diode-clamped MLI'S were developed followed by flying capacitor MLI'S. These three topologies utilise different mechanisms to produce the required output. The topology introduced first, that is, the CMLI, is simply series connection of H-bridges. The diode-clamped MLI uses series capacitor bank whereas, in flying capacitor mli, floating capacitors are used in order to clamp the output voltage [1]. H-bridge inverters have isolation transformers, and then H-bridge cascaded MLIS were introduced to separate DC input sources. But they do not need either clamping a diode or flying capacitors. Absence of voltage imbalance is the main advantage of cascaded multi. Fewer components are used in CMLI compared to diode-clamped and flying capacitor mlis [2–4].

Most of the researches are carried out in cascaded MLI configuration. But still the new trends are involved in the evolution of renewed multilevel inverters. Modifications are made in its inbuilt structure. A 7-level MLI was generated with 9 switches reducing 3 switches from the main conventional CMLI [5]. It offers good results yielding desired a 7-level output with low THD. A 7 level MLI with 7 switches reducing 2 more switches from the previous topology made a far improvement

in the investigation of the switch reduction [6]. Yet another topology of 7-level MLI was configured with 4 dc sources and just 6 switches to get 7-level output [7]. The latter made a drastic move in topology development since the THD is low, and gate circuits used to drive the switches are less.

It is mentioned everywhere that simplicity is the main advantage of CMLI to generate 5 levels using 8 switches, 7 levels with 12 switches, 9 levels with 16 switches, and so on [2–4, 8]. It clearly reveals that an increase in levels demands more number of switches. Then the comment on simplicity of CMLI is simply contradictory. Hence, the focus was eyeing on a real solution to this problem, that is, how to simplify the complex circuit. Then arise the concept of "switch reduction". Exploring the existing topologies on basic 7 level, switch reduction was made from 12 switches to 9, gradually to 7 and then to 6.

II. CONVENTIONAL TOPOLOGY

Using 3 DC voltage sources,H-bridge units each with 4 switches together forming 12 switches in total are used in conventional CMLI which is represented in Figure 1. General expression for output voltage levels, = (+2)/2where is the number of switches in the configuration. Each Bridge is outputting 3 Levels, +*V*dc, 0, −*V*dc.Cascading 3 Bridges in such a fashion to produce stepped7 level staircase waveforms.represent the switching scheme for the proposed topology.

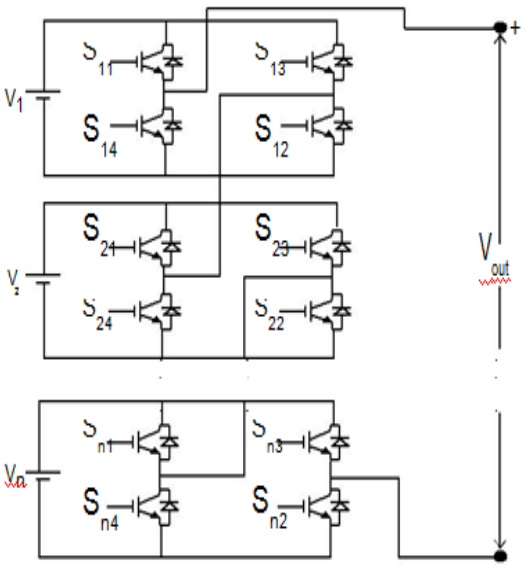

Fig 1. conventional cascaded n level MUL

Proposed Five-Switch Topology

The proposed 7 level MLI as shown in Figure 5 is about redesigning of existing 6-switch topology eliminating 1 switch attaining the tag of 5 switch configuration. The circuit thus obtained is the simplest design compared to conventional and all other existing topologies. It consists of four dc sources of 7 levels, for 9-level, 5 dc sources and so on.

Generalised expression for output voltage levels for the new topology proposed is =(2∗ −3), where =number of output voltage levels, =number of switches =(2∗V − 1), where
V =number of dc sources.

The design of pulse generation circuit makes the topology differ from others so as to obtain the unique pulse pattern to trigger the switches at the proper instant. Switches *S*1, *S*2, and *S*3 need to be compulsorily unidirectional or else the outputwaveform will get distorted. Reduced switches make the circuit compact and user-friendly. Though the usage of 4 dc sources for the generation of 7-level MLI results in less utilisation of sources, switch reduction benefits in low switching losses. No H-Bridge is used.

III. EXISTING TOPOLOGY

7-Level, 6 Switches**.** This is a special configuration consisting of four dc sources and six switches. One switch across the load is used for zero level. *S*1, *S*2, *S*3 used for level generation and *S*4, *S*5 switches for polarity changing Figure 1 represent the 7-level 6-switch topology and the corresponding switching

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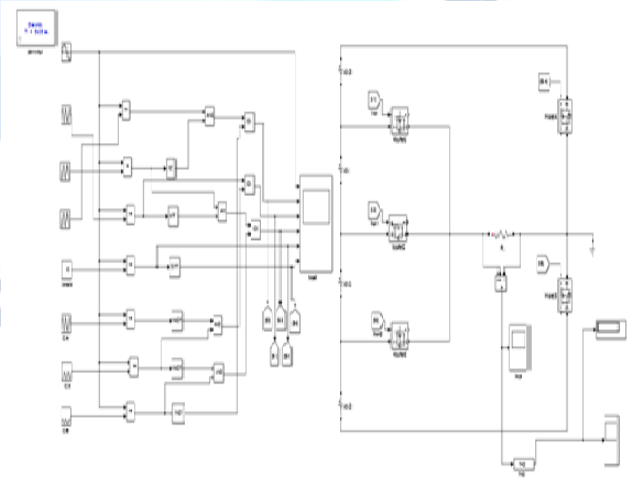

Fig 2. 7level, 6 switches

Table 1: 7 level 6 switch

SL no.	1	2	3	4	5	6	Output voltage
1	OFF	OFF	ON	OFF	ON	OFF	+Vdc
2	OFF	ON	OFF	OFF	ON	OFF	+2Vdc
3	ON	OFF	OFF	OFF	ON	OFF	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	ON	0
5	ON	OFF	OFF	ON	OFF	OFF	−Vdc
6	OFF	ON	OFF	ON	OFF	OFF	−2Vdc
7	OFF	OFF	ON	ON	OFF	OFF	−3Vdc

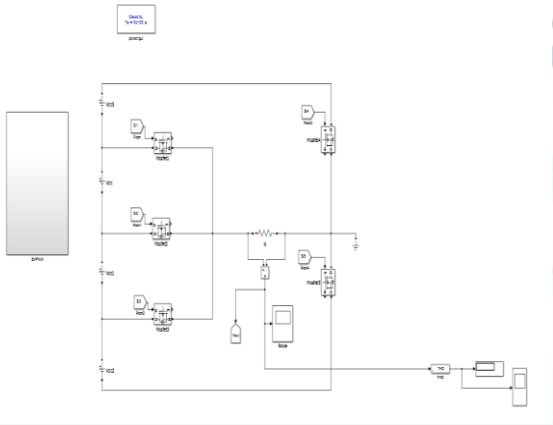

Fig 3. 7level, 5 switches

Table 2: 7 level 5 switch

SL no.	1	2	3	4	5	Output voltage
1	OFF	OFF	ON	OFF	ON	+Vdc
2	OFF	ON	OFF	OFF	ON	+2Vdc
3	ON	OFF	OFF	OFF	ON	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	0
5	ON	OFF	OFF	ON	OFF	−Vdc
6	OFF	ON	OFF	ON	OFF	−2Vdc
7	OFF	OFF	ON	ON	OFF	−3Vdc

IV. HARDWARE RESULTS

The proposed inverter is digitally implemented in *Universal VLSI Moon1* board. The board has X*C3S400PQ208* FPGA device as the main feature consists of 400k system gates, 8,064 logic cells, 896 CLBs,264 maximum user I/Os. Other features used on the *Universal VLSI Moon1* board are a 4 MHz oscillator for clock source, one pushbutton switch for system reset and toggle switches for the selection of modulation index values. For the generation of PWM it is required to compare the sinusoidal modulating signal and the triangular carrier signal. A simple logic which I have used is the "COUNTER". The pulse width depends on the counter speed. The count is nothing but the input data which will be variable. If the counter speed is slow then the width of the pulse is more and if it counts fast the short width pulse will be generated. The speed of the counter depends on the clock. This clock is nothing but the system clock which I will use as sinusoidal modulating signal. The system clock is high frequency near about 4 MHz to 6 MHz. By using "divide by" network required modulating signal can be obtained.

The following figure shows the flow how the seven PWM pulses are generated.

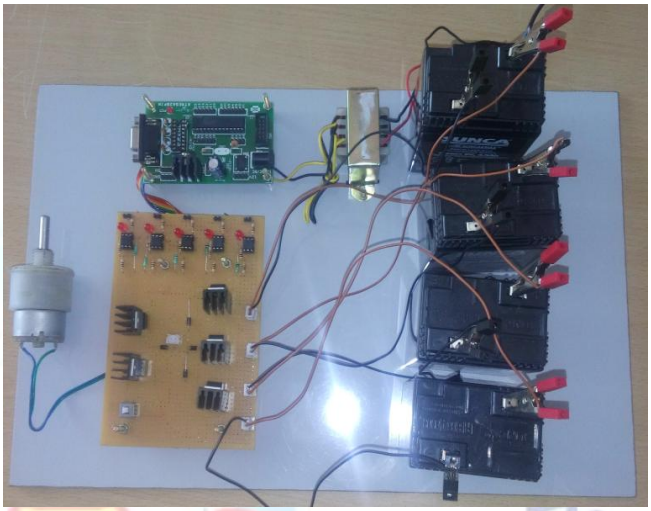

Fig 4. Hardware setup

The model of the proposed multilevel PWM single phase inverter is simulated by using Xilinx simulation tool. The PWM pattern is derived and simulated at different modulation indexes (Ma) as a control signals; the system is tested and simulated by resistive.

V. CONCLUSION

The simulation results of the multilevel inverter for various levels using),phase opposition disposition (POD) methods simulated using MATLAB/Simulink software and got lower total harmonic distortion (THD) in phase opposition disposition(POD) method than other techniques in multicarrier pulse width modulation(MCPWM) and the results are tabulated.

The space vector pulse width modulation (SPVPWM) with space vector reference wave technique is implemented in the reduced the lower order harmonics like 3rd, 5th and 7th .the POD method in THD (23.4%) to reduce the space vector pulse with modulation the harmonic were reduced in (3.95)%.

By comparing with the space vector reference wave technique and selective harmonic elimination techniques, it shows that the Selective harmonic elimination technique has very low THD than other techniques. Thus, the hardware implementation is carried out for seven-level inverter with particle swarm optimization technique using

microcontroller and the output results are observed.

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