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Leakage Current Calculation for PV Inverter System Based on a Parasitic Capacitor Model

S.Thakkalai Peer Mohamed[1] | V.Ashok Kumar[2]

[1]Department of EEE, Roever Engineering College, Perambalur, Tamilnadu, India.
[2]Assistant Professor, Department of EEE, Roever Engineering College, Perambalur, Tamilnadu, India.

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ABSTRACT

Considering low efficiencies of solar panels, the dependability and efficiency of power electronic interface has to be ensured. Transformer less PV inverters increases the efficiency by nearly 2 percentage and decrease cost by 25 percentages. With no galvanic isolation comes the problem of dc injection and ground leakage current which pauses serious problems to core saturation of distribution transformers, cable corrosion, Power quality and EMI problems and has to be limited as per IEEE standards. This paper gives an analysis of leakage current flowing through the parasitic capacitance and also the DC injection in the output of the inverter. Analysis is done for various values of parasitic capacitance. Five different Bridge derived topologies and PWM techniques are evaluated On the basis of leakage current and DC injection.

KEYWORDS: *DC injection, Common Mode Voltage, Differential Mode Voltage, Parasitic Capacitance, Leakage current.*

I. INTRODUCTION

Avoiding transformers while connecting PV inverters to grid has gained much popularity due to its increased efficiency (nearly by 2%) and decreased cost (nearly by 25%). Transformers used for isolation could either be line frequency transformers which increase the bulkiness of the system while high frequency transformers require more than one power stage and increase system complexity. However, transformer less inverter have a serious drawback of ground leakage current which flows between the PV array and the ground through the parasitic capacitance that exists between PV cell and its frame. When the frame is grounded the parasitic capacitance exists between the PV array and ground. The common mode voltage fluctuations across this capacitance cause ground leakage current flow which initiates problems of EMI, personnel safety, power quality issues and system losses. Large ground leakage currents are formed when parasitic capacitance AC side filter inductors and grid form a resonant circuit.

In the past few years, there have been many research publications [1-3] demonstrated to study this parasitic parameter. The stray parameter related issues can be defined into two groups. There are single capacitor model [15], [4-9] and multi conductor array model. To minimize the leakage current, the maintenance of constant common mode voltage is primarily required. The whole PV array can be represented as one capacitor from the DC bus to the ground. Because of its clarity, this model is generally used in the leakage current analysis, modulation technique improvement [10], and new inverter topology implementations. Paper [12-14] believes the value of this capacitance depends upon the size of the module, the height above the ground, and the relative humidity that affects the dielectric permittivity of air Common mode voltage largely depends on topology of the inverter and PWM techniques [11]. Full bridge configuration with bipolar PWM has constant common mode voltage but with a reduced efficiency and large output current ripple. Full bridge with unipolar PWM has many advantages of increased efficiency and three level output. There are other full bridge derived structures like H5 and HERIC topologies which use additional switches for DC and AC decoupling respectively. Decoupling switches enable the disconnection of PV panel from the grid during freewheeling modes. This helps in limiting the DC link voltage ripple.

II. Capacitance Modeling

The silicon cell is packaged in a sandwich structure with such encapsulated material as glass, Ethylene-vinyl acetate (EVA), back sheet (Tedlar) and aluminium frame. The silicon cell acts as one conductor while the panel frame, the mounting rack or the ground constructs the other conductor of the capacitor. Therefore, the parasitic capacitances in PV panel are split into three parts in this paper. (A) Cell-to-frame capacitance Ccf, (B) Cell-to-rack capacitance Ccr and (C) Cell-to-ground capacitance Ccg.

2.1 Cell-to-frame capacitance

Cell-to-frame capacitance is between the PV silicon cell and its aluminium frame. Although the effective surface area of this capacitor is not very large, the distance between the capacitor plates (silicon cell and its aluminium frame) is very small. So, this capacitance could not be neglected at the beginning of our study. Since the structure of a PV module is comparatively fixed after a commercial manufacture procedure, it is not difficult to understand that the value of *C*CF should be independent on the type of mounting. And, it may have certain relations to the inner material and structure of the PV panel.

2.2 Cell- to-rack capacitance

Cell- to-rack capacitance is between the PV silicon cell and its mounting rack. Since there are lots of different types of rack, the value of *C*cr various with the structure, size and shape of racks. And due to the length limitation of the manuscript, the capacitance of only one simple rack structure is analyzed and calculated in this paper.

2.3 Cell-to-ground

Cell-to-ground capacitance is generally considered to be the main parasitic parameter in PV panel, since the effective surface area of *C*cg is larger than the other two parasitic capacitances without a doubt. However, the effective electrode distance of *C*cg (between panel and ground) is usually far away, when compared with the effective electrode distance of *C*cf (between silicon cell and its aluminium frame). What's more, for two commonly used mounting methods, i.e. building integrated mounting method and shade structure mounting method, the distance between panel and ground is different from each other. The former distance is very close while the latter distance is far away.

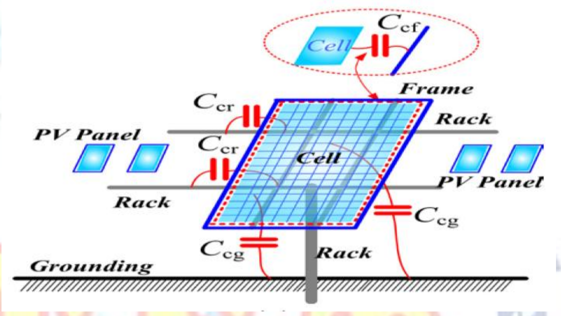

Fig.1.Capacitance Model

III. Existing System

When a galvanic connection between the grid and the PV array is made, a common-mode voltage exists which generates common-mode currents. These common-mode currents may produce electromagnetic interferences, grid current distortion and additional losses in the system. Therefore, to avoid the leakage currents that would penalize the transformer less power chains, it is worth focusing on topologies which do not generate common-mode currents. Some topologies available in the market touch more or less such a crucial requirement. However, some drawbacks generated by the non-utilization of the line transformer still exist. This is said, a small room for improvement still exists. The first goal of this reviews to focus on recently developed topologies which do not generate common-mode voltage

3.1 Block diagram

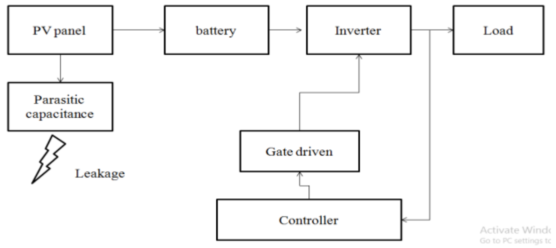

Fig.2.Existing block diagram

In this method normal parasitic capacitance is used to ground the leakage current. Only gate driven unit is used to control the inverter. PI control is used to control the output of the inverter.

IV. Proposed System

In order to achieve the constant common mode voltage to eliminate the leakage current, a new modulation strategy is proposed cell-to-frame capacitance Ccf, cell-to-rack capacitance Ccr cell-to-ground capacitance Ccg

4.1 Proposed block diagram

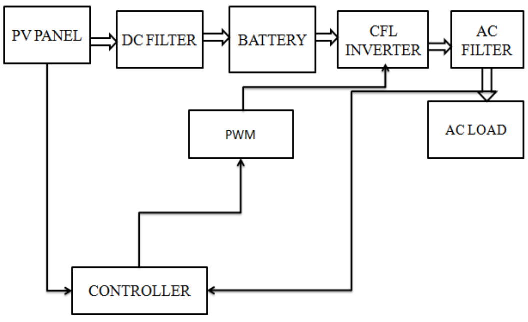

Fig.3.Proposed block diagram

4.2 Proposed circuit diagram

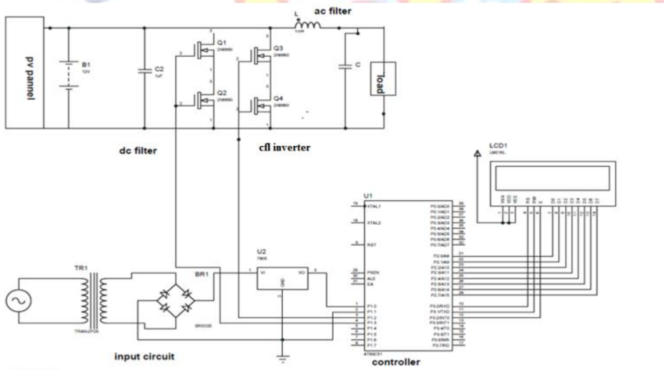

Fig.4.Existing circuit diagram

MPPT control is used in microcontroller to control to track the panel voltage. Controller is used to compare the reference voltage and normal load voltage. Gate driven unit is used to control the on and off time of the Inverter.

V. System Description

5.1 PV panel

Fig.5.Photovoltaic panel

Photovoltaic's (PV) is a method of generating electrical power by converting sunlight into direct current electricity using semiconducting materials that exhibit the photovoltaic effect.

A photovoltaic system employs solar panels composed of a number of solar cells to supply usable solar power.

5.2 PWM

Pulse Width Modulation, or PWM, is a technique for getting analog results with digital means. Digital control is used to create a square wave, a signal switched between on and off. This on-off pattern can simulate voltages in between full on (5 Volts) and off (0 Volts) by changing the portion of the time the signal spends on versus the time that the signal spends off. The duration of "on time" is called the pulse width modulation.

Fig.6.Photo of PV inverter

Charging a battery with a solar system is a unique and difficult challenge. In the "old days," simple on-off regulators were used to limit battery outgassing when a solar panel produced excess energy. However, as solar systems matured it became clear how much these simple devices interfered with the charging process. The history for on-off regulators has been early battery failures, increasing load disconnects, and growing user dissatisfaction. PWM has recently surfaced as the first significant advance in solar battery charging.

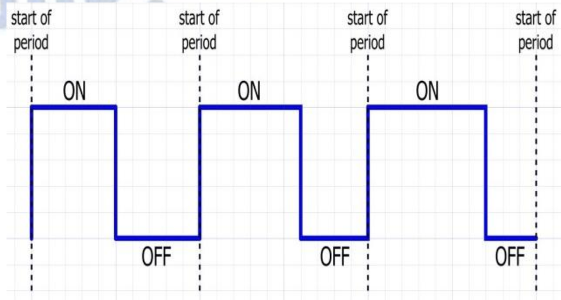

Fig.7.On-off period pwm

VI. Simulation Verifications

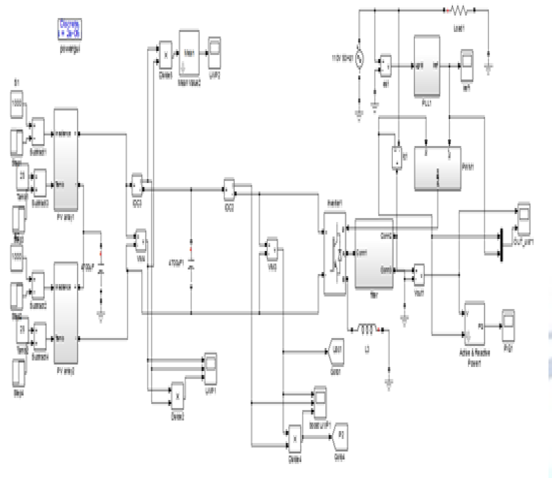

Fig.8.Simulation of pv inverter

A. Inverted voltage

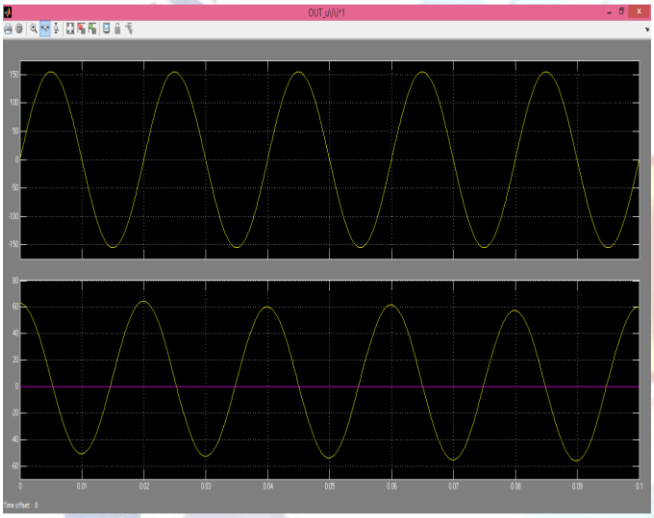

Fig.9.Inverter voltage

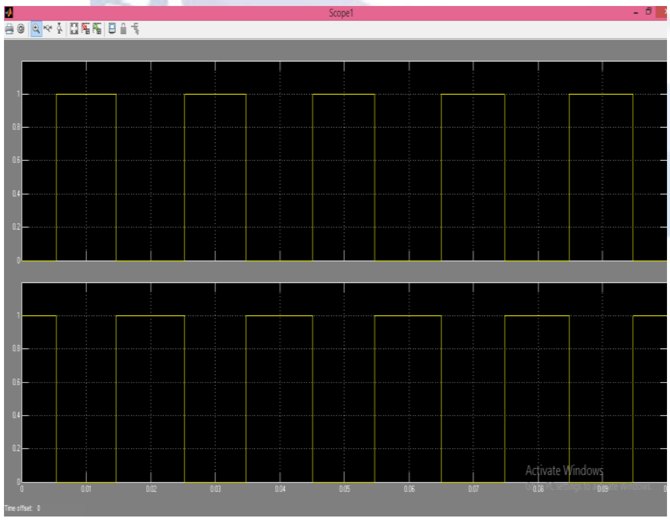

Fig.10.Output of pwm pulse

VII. Conclusion

This paper presented the analysis of the leakage current occurrence in CMI based PV system caused by the removal of transformer. This leakage current issue features the intermodule leakage current loop among the inverter module. This leakage current is reduced using filter based suppression solution by constructing LC filter at circulating current paths. The modified H-bridge inverter is attenuating high frequency noises. The analytical method was used to reduce leakage current issue by utilizing the low capacitance, and parasitic capacitor for high switching frequency

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