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Reduction of Power Electronic Devices with a New Basic Unit for a Cascaded Multilevel Inverter fed Induction Motor

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ABSTRACT

In this paper, a new cascaded multilevel inverter by capability of increasing the number of output voltage levels with reduced number of power switches is proposed. The proposed topology consists of series connection of a number of proposed basic multilevel units. Multilevel inverters have an attracted a great deal of attenuation in medium voltage and high power application Due to their lower switching losses, EMI, high efficiency. This paper proposes to Cascade H bridge multilevel inverter to reduced total harmonic Distortion by increase the output voltage level. In this paper single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit with Reduced Number of Power Switches fed induction motor. Thus multilevel inverter topologies are becoming more popular. A multilevel inverter topology is discussed. The inverter consists of series connection of a number of basic units. Therefore, multilevel inverters had been introduced and are being developed now. With an increasing number of dc voltage sources in the input side, a sinusoidal like waveform can be generated at the output. As a result, the total harmonic distortion (THD) decreases, and the output waveform quality increases, which are the two main advantages of multilevel inverters. In addition, lower switching losses, lower voltage stress of dv/dt on switches, and better electromagnetic interference are the other most important advantages of multilevel inverters. These features are obtained by the comparison of the conventional cascaded multilevel inverters with the proposed cascaded topology. The ability of the proposed inverter to generate all voltage levels (even and odd) is reconfirmed by using the simulation results of a 15-level inverter and single phase 15-level inverter fed induction motor. Induction motors are widely used in industries, because they are rugged, reliable and economical. Induction motor drive requires suitable converters to get the required speed and torque without or negligible ripples. The simulation results are presented by using Matlab/Simulink Model.

KEYWORDS: *Basic unit, cascaded multilevel inverter, developed cascaded multilevel inverter, H-bridge, Induction motor.*

I. INTRODUCTION

Nowadays, the multilevel inverters have received much attention because of their considerable advantages such as high power quality, lower harmonic components, better electromagnetic consistence, lower dv/dt, and lower switching losses [1]. There are three main types of multilevel inverters: diode clamp multilevel inverter, flying

capacitor multilevel inverter, and cascaded multilevel inverter [2]. The cascaded multilevel inverters have received special attention due to the modularity and simplicity of control. The cascaded multilevel inverters are mainly classified into two groups:1) symmetric, with equal magnitude for the dc voltage sources; and 2) asymmetric, with different values of the dc voltage sources. By increasing the magnitude of dc voltage sources, the higher number of output levels will be generated. Therefore, the asymmetric cascaded multilevel inverters increase the number of output levels by using power semiconductor devices that are the same as the symmetric ones [3]. Up to now, different topologies with several algorithms to determine the magnitude of their dc voltage sources have been presented in the literatures. In [4], the H-bridge cascaded multilevel inverter with two different algorithms as symmetric and asymmetric inverters has been presented. Two other symmetric cascaded multilevel inverters have been also presented in [5]. The main advantage of these inverters is the low number of different voltage amplitudes of the used dc sources. However, the higher number of required insulated gate bipolar transistor (IGBTs), power diodes, and driver circuits in generating a specific output level are their remarkable disadvantages. In order to increase the number of output levels with a lower number of power semiconductor devices, different asymmetric cascaded multilevel inverters have been presented in [6].The bidirectional power switches have been used in these topologies. Each bidirectional power switch includes two IGBTs, two power diodes, and one driver circuit if the common emitter configuration is used. Therefore, in these topologies,the installation space and total cost of the inverter increase [7]. As a result, several asymmetric cascaded multilevel inverters have been presented in which the unidirectional switches from the voltage point of view and the bidirectional switches from the current point of view are used in them. Each unidirectional switch consists of an IGBT with an anti-parallel diode. Two of these topologies have been presented in [8] and [9]. Two other algorithms for the H-bridge cascaded multilevel inverter have been also presented in [10] and [11].

In this paper, the topology proposed is single phase fifteen- level cascaded multilevel H bridge inverter for three phase grid connected system. A fifteen level cascaded multilevel H bridge inverter to reduce the Total Harmonic Distortion (THD)of the inverter output voltages for single phase induction motor system are presented [12-13].

A multilevel inverter consists of a series of H-bridge inverter units connected to single phase induction motor. The general function of this multilevel inverter is to synthesize a desired voltage from several DC sources. The AC terminal voltages of each bridge are connected in series.

II. PROPOSED TOPOLOGY

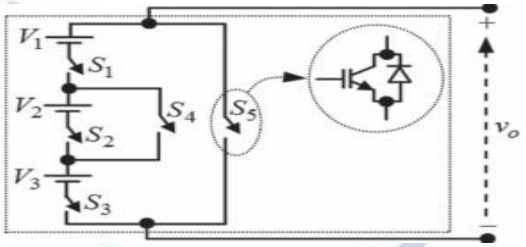

Fig. 1. Proposed basic unit.

TABLE I

Permitted Turn On and Off States forSwitches in the Proposed Basic Unit

state	Switches state					v_o
	S_1	S_2	S_3	S_4	S_5	
1	off	off	off	off	on	0
2	on	off	on	on	off	V_1+V_3
3	on	on	on	off	off	$V_1+V_2+V_3$

Fig. 1 shows the proposed basic unit. As shown in Fig. 1, the proposed basic unit is comprised of three dc voltage sources and five unidirectional power switches. In the proposed structure, power switches (S2, S4), (S1, S3, S4, S5), and (S1, S2, S3, S5) should not be simultaneously turned on to prevent the short circuit of dc voltage sources. The turn on and off states of the power switches for the proposed basic unit are shown in Table I, where the proposed basic unit is able to generate three different levels of 0, V1 + V3, and (V1 + V2 +V3) at the output. It is important to note that the basic unit is only able to generate positive levels at the output.

It is possible to connect n number of basic units in series. As this inverter is able to generate all voltage levels except V1, it is necessary to use an additional dc voltage source with the amplitude of V1 and two unidirectional switches that are connected in series with the proposed units. The proposed cascaded inverter that is able to generate all levels is shown in Fig. 2(a). In this inverter, power switches S'1 and S'2 and dc voltage source V1 have been used to produce the lowest output level. The amplitude of this dc voltage source is considered V1 = Vdc (equal to the minimum output level). The output voltage level of each unit is

indicated by Vo, 1, Vo, 2, . . . , Vo, n, and V'o. The output voltage level vo of the proposed cascaded multilevel inverter is equal to

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \cdots + v_{o,n}(t) + v'_o(t) \quad (1)$$

The generated output voltage levels of the proposed inverter are shown in Table II. As aforementioned and according to Table II, the proposed inverter that is shown in Fig. 2(a) is only able to generate positive levels at the output.

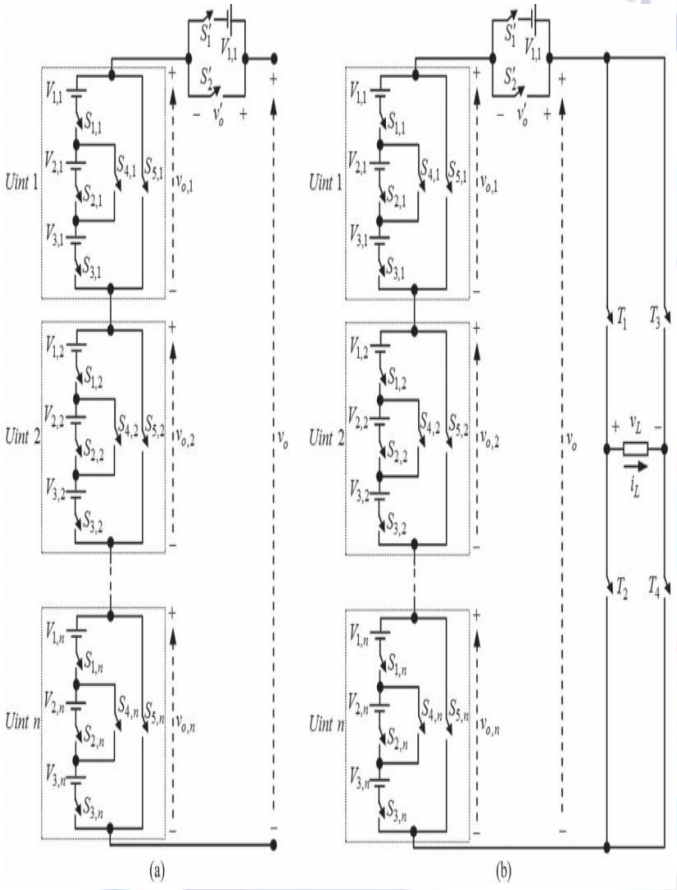

Fig. 2. Cascaded multilevel inverter. (a) Proposed topology. (b) Developed proposed topology.

TABLE II
Generated Output Voltage Levels Vo Based On the Off And On States of Power Switches

v_o	S'_1	S'_2	$S_{1,1}$	$S_{2,1}$	$S_{3,1}$	$S_{4,1}$	$S_{5,1}$	$S_{1,2}$	$S_{2,2}$	$S_{3,2}$	$S_{4,2}$	$S_{5,2}$	...	$S_{1,n}$	$S_{2,n}$	$S_{3,n}$	$S_{4,n}$	$S_{5,n}$
0	off	on	off	off	off	off	on	off	off	off	off	on	...	off	off	off	off	on
V_1	on	off	off	off	off	off	on	off	off	off	off	on	...	off	off	off	off	on
$V_{1,1}+V_{3,1}$	off	on	on	off	on	on	off	off	off	off	off	on	...	off	off	off	off	on
$V_{1,1}+V_{2,1}+V_{3,1}$	off	on	on	on	on	off	off	off	off	off	off	on	...	off	off	off	off	on
$V_{1,2}+V_{3,2}$	off	on	off	off	off	off	on	on	off	on	on	off	...	off	off	off	off	on
$V_{1,2}+V_{2,2}+V_{3,2}$	off	on	off	off	off	off	on	on	on	on	off	off	...	off	off	off	off	on
$V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,3}$	off	on	on	on	on	off	off	on	off	on	on	off	...	off	off	off	off	on
$V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,2}+V_{2,3}$	off	on	on	on	on	off	off	on	on	on	off	off	...	off	off	off	off	on
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$\sum_{j=1}^{n}(V_{1,j}+V_{2,j}+V_{3,j})$	off	on	on	on	on	off	off	on	on	on	off	off	...	off	off	off	off	on
$V_{1,1}+\sum_{j=1}^{n}(V_{1,j}+V_{2,j}+V_{3,j})$	on	off	on	on	on	off	off	on	on	on	off	off	...	off	off	off	off	on

TABLE III
Proposed Algorithms and Their Related Parameters

Proposed algorithm	Magnitude of dc voltage sources	N_{level}	$V_{o,max}$	V_{block}
First proposed algorithm (P_1)	$V_{1,j}=V_{2,j}=V_{3,j}=V_{dc}$ for $j=1,2,\cdots,n$	$6n+3$	$(3n+1)V_{dc}$	$(21n+6)V_{dc}$
Second proposed algorithm (P_2)	$V_{1,1}=V_{2,1}=V_{3,1}=V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=2V_{dc}$ for $j=2,3,\cdots,n$	$12n-3$	$6n-2$	$(40n-13)V_{dc}$
Third proposed algorithm (P_3)	$V_{1,1}=V_{2,1}=V_{3,1}=V_{dc}$ $V_{1,j}=\frac{1}{3}V_{2,j}=V_{3,j}=3^{j-2}V_{dc}$ for $j=2,3,\cdots,n$	$5(3^{n-1})+4$	$\left[\frac{5(3^{n-1})+3}{2}\right]V_{dc}$	$[82(3^{n-1})-7]V_{dc}$
Fourth proposed algorithm (P_4)	$V_{1,j}=0.5V_{2,j}=V_{3,j}=2^{j-1}V_{dc}$ for $j=1,2,\cdots,n$	$2^{n+3}-5$	$(2^{n+2}-3)V_{dc}$	$[7(2^{n+2})-22]V_{dc}$

Therefore, an H-bridge with four switches T1–T4 is added to the proposed topology. This inverter is called the developed cascaded multilevel inverter and is shown in Fig. 2(b). If switches T1 and T4 are turned on, load voltage vL is equal to vo, and if power switches T2 andT3 are turned on, the load voltage will be −vo. For the proposed inverter, the number of switches Nswitch and the number of dc voltage sources Nsource are given by the following equations, respectively,

$$N_{\text{switch}} = 5n + 6 \quad (2)$$

$$N_{\text{source}} = 3n + 1 \quad (3)$$

Where n is the number of series-connected basic units. As the unidirectional power switches are used in the proposed cascaded multilevel inverter, the number of power switches is equal to the numbers of IGBTs, power diodes, and driver circuits. The other main parameter in calculating the total cost of the inverter is the maximum amount of blocked voltage by the switches. If the values of the blocked voltage by the switches are reduced, the total cost of the inverter decreases [12]. Inaddition, this value has the most important effect in selecting the semiconductor devices because this value determines the voltage rating of the required power devices. Therefore, in order to calculate this index, it is necessary to consider the amount of the blocked voltage by each of the switches. According to Fig. 2(b), the values of the blocked voltage by switches are equal to

$$V_{S'1} = V_{S'2} = V_{1,1} \quad (4)$$

$$V_{S1,j} = V_{S3,j} = \frac{V_{1,j} + V_{2,j} + V_{3,j}}{2} \quad (5)$$

$$V_{S4,j} = V_{S2,j} = V_{2,j} \quad (6)$$

$$V_{S5,j} = V_{1,j} + V_{2,j} + V_{3,j} \quad (7)$$

$$V_{T1} = V_{T2} = V_{T3} = V_{T4} = V_{o,\max} \quad (8)$$

Where Vo, max is the maximum amplitude of the producible output voltage. Therefore, the maximum amount of the blocked voltage in the proposed inverter Vblock is equal to

$$V_{\text{block}} = \sum_{j=1}^{n} V_{\text{block},j} + V'_{\text{block}} + V_{\text{block,H}} \quad (9)$$

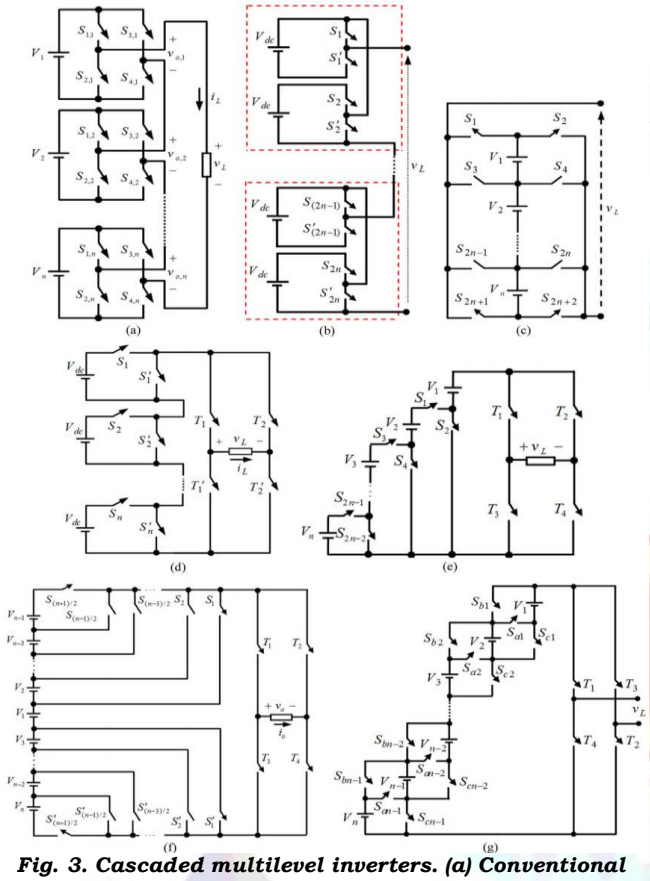

Fig. 3. Cascaded multilevel inverters. (a) Conventional cascaded multilevel inverter R2 for V1 = V2 = · · · = Vn = Vdc, R3 for V1 = Vdc, V2 =· · · = Vn = 2Vdc [12], and R4 for V1 = Vdc, V2 = · · · = Vn = 3Vdc. (b) Presented topology, with R7 for V1 = V2 = · · · = Vn = Vdc. (c) Presented topology, with R8 for V1 = V2 = · · · = Vn = Vdc and R9 for V1 = Vdc, V2 = · · · = Vn = 2Vdc. (d) Presented topology with R10. (e) Presented topology with R6 for V1 = V2 = · · · =Vn = Vdc. (f) Presented topology with R5 for V1 = V2 = · · · = Vn =Vdc.(g) Presented topology in [13], with R1 for V1 = V2 = · · · = Vn = Vdc.

In (9), Vblock,j, Vblock , and Vblock, H indicate the blocked voltage by the jth basic unit, the additional dc voltage sources, and the used H-bridge, respectively.

In the developed inverter, the number and maximum amplitude of the generated output levels are based on the value of the used dc voltage sources. Therefore, four different algorithmsare proposed to determine the magnitude of the dc voltage sources. These proposed algorithms and all their parameters are calculated and shown in Table III. According to the fact that the magnitudes of all proposed algorithms except the first algorithm are different, the proposed cascaded multilevel inverter based on these algorithms is considered an asymmetric cascaded multilevel inverter. In addition, based on the equations of the maximum output voltage levels and its maximum amplitude, it is clear that these values in the asymmetric cascaded multilevel inverter are more than those in the symmetric cascaded multilevel inverters with the same number of used dc voltage sources and power switches.

III. COMPARING THE PROPOSED TOPOLOGY WITH THE CONVENTIONAL TOPOLOGIES

The main aim of introducing the developed cascaded inverter is to increase the number of output voltage levels by using the minimum number of power electronic devices. Therefore, several comparisons are done between the developed proposed topology and the conventional cascaded inverters from the numbers of IGBTs, driver circuits, and dc voltage sources points of view. In addition, the maximum amount of the blocked voltage by the power switches is also compared between the proposed inverter and the other presented topologies. In this comparison, the proposed cascaded inverter that is shown in Fig. 2(b) with its proposed algorithms is represented by P1 to P4, respectively. In [13], a symmetric cascaded multilevel inverter has been presented that is shown by R1 in this comparison. The H-bridge cascaded multilevel inverter has been presented. This inverter is represented by R2. In addition, two other algorithms have been presented for the H-bridge cascaded inverter in [12] and that are representedby R3 and R4, respectively. In, three other symmetric cascaded multilevel inverters have been presented.

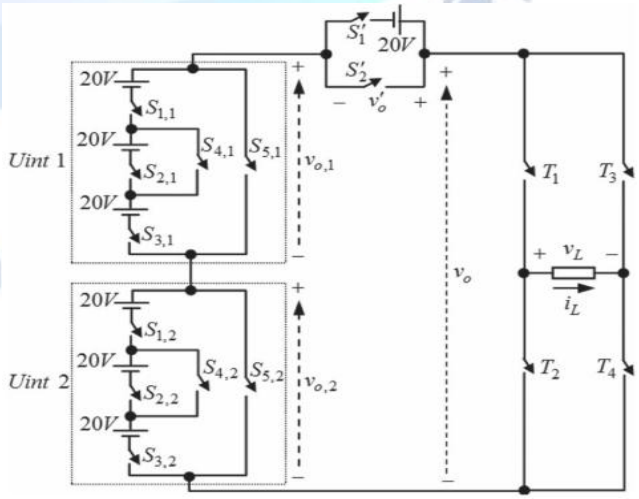

Fig. 4. Cascaded 15-level inverter based on the proposed basic unit.

These inverters are shown by R5–R7, respectively. The other cascaded multilevel inverter with two different algorithms has been presented. This inverter with its algorithms is represented by R8 and R9, respectively. Another symmetric cascaded multilevel inverter that has been presented is represented by R10 in this comparison. Fig. 3 indicates all of the aforementioned cascaded multilevel inverters. In this section, the investigations are done on a cascaded multilevel inverter thatis shown in Fig. 4. This inverter consists of two proposed basicunits and one additional series-connected dc voltage source that lead to the use of 7 dc voltage sources and 12 unidirectional power switches. The first proposed algorithm is considered to determine the magnitude of the dc voltage sources with Vdc =20 V. According to (5), this inverter is able to generate 15 levels (seven positive levels, seven negative levels, and one zero level) with the maximum amplitude of 140 V at the output.

It is important to note that the load is assumed as a resistive–inductive (R–L) load, with R=70 Ω, and L=55 mH. It is important to point out that the used control method in this inverter is the fundamental control method. The main reason to select this control method is its low switching frequency compared with other control methods that leads to reduction in switching losses.

IV.INDUCTION MOTOR

Induction Motor (1M) An induction motor is an example of asynchronous AC machine, which consists of a stator and a rotor. This motor is widely used because of its strong features and reasonable cost. A sinusoidal voltage is applied to the stator, in the induction motor, which results in an induced electromagnetic field. A current in the rotor is induced due to this field, which creates another field that tries to align with the stator field, causing the rotor to spin. A slip is created between these fields, when a load is applied to the motor.
Compared to the synchronous speed, the rotor speed decreases, at higher slip values. The frequency of the stator voltage controls the synchronous speed [12]. The frequency of the voltage is applied to the stator through power electronic devices, which allows the control of the speed of the motor. The research is using techniques, which implement a constant voltage to frequency ratio. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$n_s = \frac{120f}{p}$$

Where f is the frequency of AC supply, n, is the speed of rotor; p is the number of poles per phase of the motor. By varying the frequency of control circuit through AC supply, the rotor speed will change.

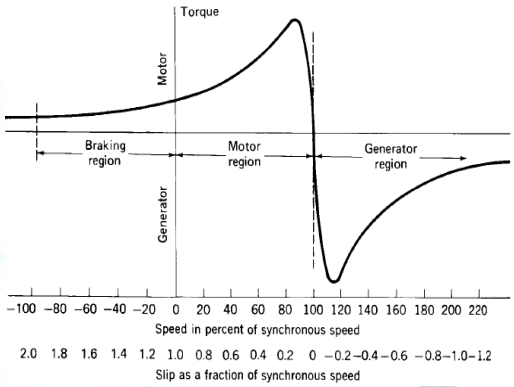

Fig.5.Speed torque characteristics of induction motor.

V.MATLAB/SIMULATION RESULTS

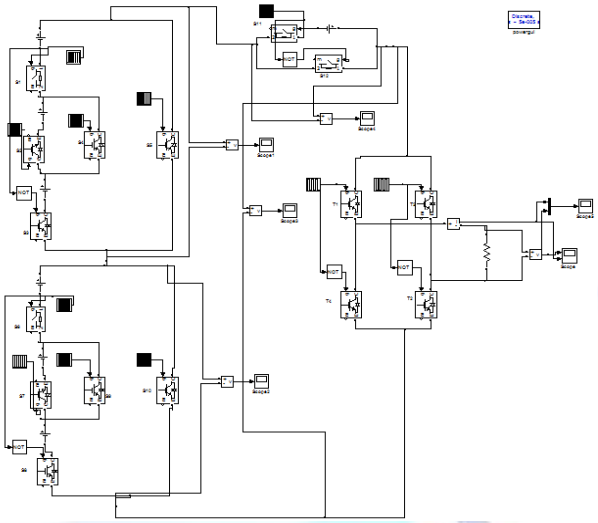

Fig.6.Matlab/Simulation Model Of Cascaded 15-Level Inverter Based On The Proposed Basic Unit.

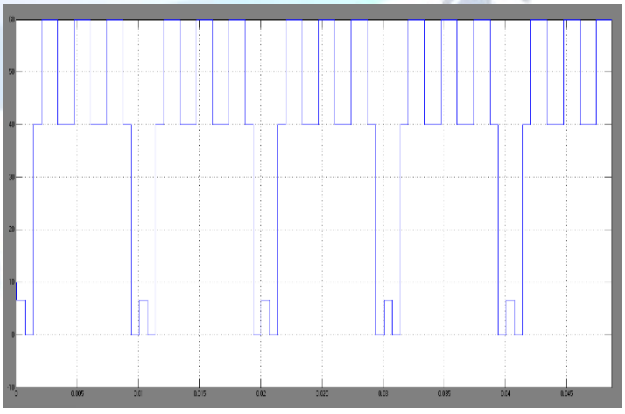

Fig.7.Proposed Basic Unit 1 of Voltage (Vo1).

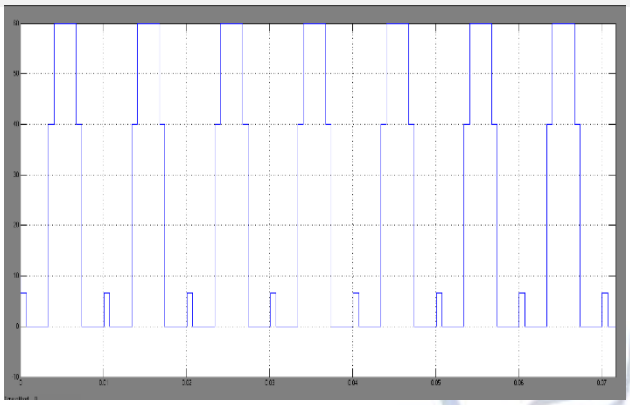

Fig.8.Proposed Basic Unit 2 of Voltage (Vo2).

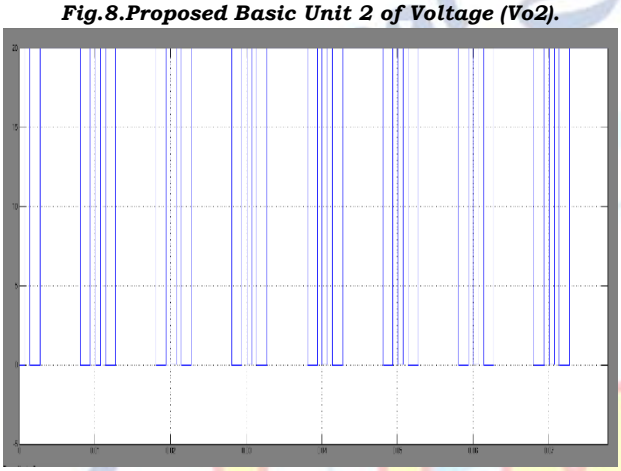

Fig.9.Output Voltage of Vo'.

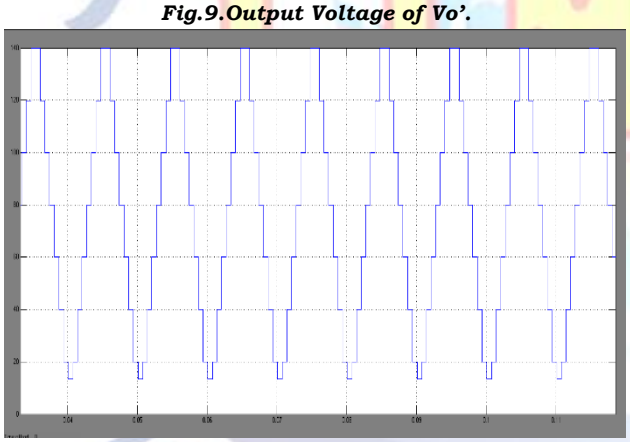

Fig.10.Voltage of Vo.

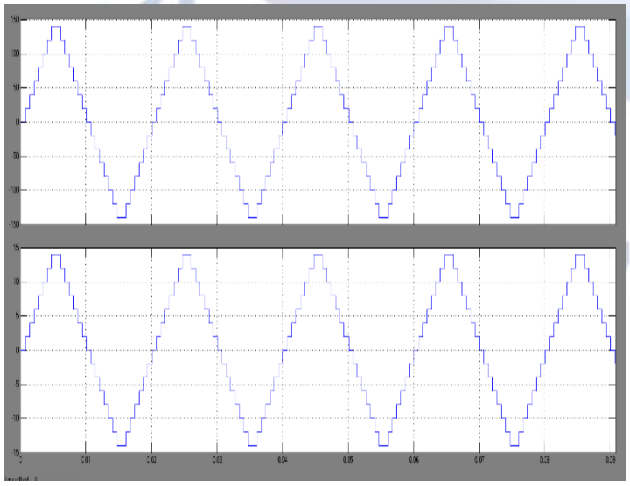

Fig.11.Output Voltage and Current of Fifteen Level Inverter.

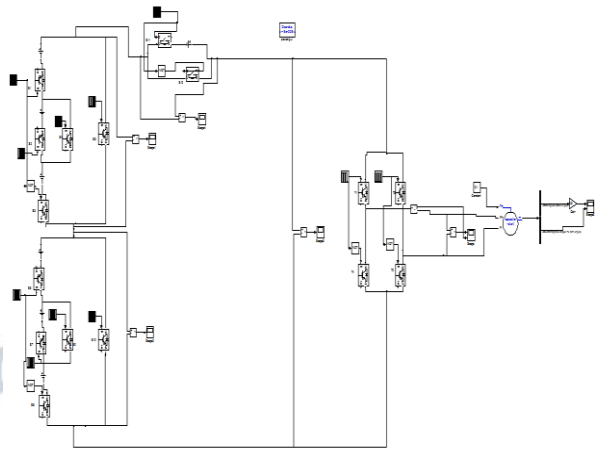

Fig.12.Matlab/Simulation Model of single phase cascaded MLI connected with Induction motor drive.

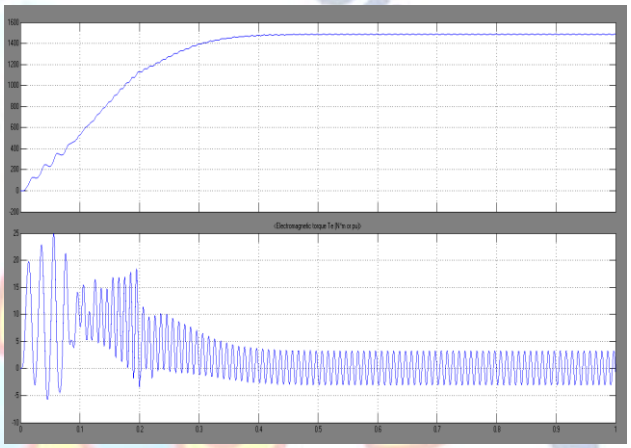

Fig.13. Speed and Torque of single Phase MLI connected with induction motor drive.

V. CONCLUSION

In this paper, a cascaded multilevel inverter based on a new basic unit is proposed. The proposed unit is only able to generate positive levels at the output. Therefore, in order to generate all voltage levels (positive and negative) the H-bridge is added to the proposed topology. The proposed inverter has the advantages of reducing the number of switches and gate drives circuits by 25 % compared with the conventional Multi-level inverter. Therefore, the proposed inverter exhibits the merits of simplified gate drive, low cost compared to the other topologies for the same number of phase voltages levels.The simulation results for 15 level cascaded inverters are presented. The three cascaded multi-level inverters have been calculated at different phase. Their speed and torque are compared. We have observed that the performance of the induction motor drive improves with increase in voltage level of the inverter. The simulation results show that the Induction Motor drives has a satisfactory performance.

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