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SEPIC Converter using Neural Network for the Enhancement of Efficiency of Multiple Output SMPS

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ABSTRACT

In this paper a new bridgeless converter for the personal computer (PC). Generally a multiple output Switched Mode Power Supply use bridgeless converter an the front end. Single phase ac supply is fed to this bridgeless converter to eliminate back to back connected buck-boost converter to reduce the size of circuit. And in the place of back to back connected buck-boost converter a Single-Ended Primary-Inductor Converter (SEPIC) is used and operate in discontinuous conduction mode (DCM) to ensure power factor correction (PFC) operation complexity of control is reduced. The performance of the proposed multiple output SMPS is improved by using feed forward algorithm of neural network and simulating the circuit in MATLAB. The obtained result from simulation are validated experimentally on a developed prototype. The proposed bridgeless converter and simulation achieve the improved performance of multiple output SMPS.

KEYWORDS: *Bridgeless buck-boost converter, DCM, Multiple output SMPS, Improved settling time, PFC*

I. INTRODUCTION

Multiple dc voltages are required for powering up different parts of a personal computer (PC) which is given by the multiple output switched mode power supply. Normally ac-dc converters which are also known as rectifier are of diodes and transistors for uncontrolled and controlled dc power. This has the demerit of poor power quality. And input ac mains and slow settling time of dc output at load end, and large size of ac and dc filters recently ,this problem has been overcome by using single ended primary inductor converter which is essentially a boost converter followed by a buck boost converter. Therefore it is similar to traditional buck boost converter, but has advantages of having non inverted output (the output has the same voltage polarity as the input).

Going through the efficiency for economic reasons and environmental concerns high efficiency across the entire load is needed. The efficiency across the entire line poses a major challenge for rectifier ac to dc converters that require power factor correction. A diode bridge rectifier followed by a boost converter has been the most commonly used PFC because of its simplicity. But the front end of boost PFC exhibits 1%-3% lower efficiency at 100V line compared to that at 230V. Another drawback of boost PFC is its front end is relatively high output voltage of 380V-400V range. This high voltage has detrimental effect on switching losses of the primary switches of dc/dc output stage and also has switching losses on the boost converter and the efficiency of its isolation

transformer. In the case of buck PFC converter operation in both continuous conduction mode(CCM) and discontinuous conduction mode (DCM) does not shape the line current around the zero crossing of the line voltage i.e. at the interval when line voltage is lower than the output voltage. It exhibits comparatively high Total Harmonic Distortion (THD) and lower power factor than the boost converter. The cascade buck-boost is consist of bridge rectifier and buck-boost converter thus with increase in power rating conduction losses will also increase. To solve the problem of conduction losses bridgeless buck-boost is proposed without input rectifier and the efficiency is increased significantly. Although the SEPIC converter has the same efficiency as bridgeless buck-boost converter but it reduces the size of circuit and the problem of undershoot and overshoot have been also minimized.

Table 1. Comparition of Buck, Boost & SEPIC Converters

CHARACTERISTICS	BOOST	BUCK-BOOST	SEPIC
Inductor position	Good	Bad	Good
Input output isolation	Difficult	Easy	Easy
Output voltage V_o	> V_m	Any	Any
Start-up capability	No, auxiliary	Inherent	Inherent
Over current control	No	Yes	Yes

II. CONTRIBUTION OF BRIDGELESS CONVERTER

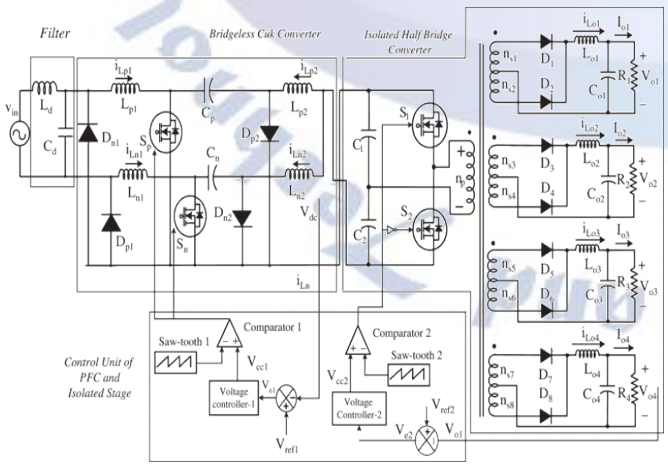


Figure 1 Circuit Configuration of Proposed Multiple Output SMPS

The ac supply is fed to the SEPIC converter which is the connection of buck-boost converter. To eliminate high frequency ripples a filter of inductor and capacitor (Lin-Cin) is connected at input end. The upper buck boost converter is consist of two diodes D_{P1} and D_{P2}, inductor L_P and conduct during the positive half cycle of ac supply consist of high frequency switch S_P. Similarly the lower buck-boost converter is consist of two diodes D_{n1} and D_{n2}, inductor L_n and conduct during negative half cycle of ac supply and has one high frequency switch S_n. To obtain inherent PFC both inductor L_P and L_n of SEPIC converter are designed in DCM. At the output of SEPIC converter the input capacitor of half bridge VSI act as the filter. The stress of voltage and current on the switches of SEPIC converter are evaluated to eliminate switch rating and heat sink design. Closed loop control is used to regulate the output dc voltage of the SEPIC converter. These regulated output voltage of SEPIC converter is fed to the half bridge VSI foe obtaining multiple dc voltage. One multiple output high frequency transformer (HFT) is used. The high frequency transformer have one primary winding and four secondary winding which are in centre tapped configuration to reduce losses.

To simulate the proposed bridgeless SEPIC converter based multiple output SMPS, it is essential to estimate components values.

III. OPERATING PRINCIPLE OF SEPIC CONVERTER BASED MULTIPLE OUTPUT SMPS

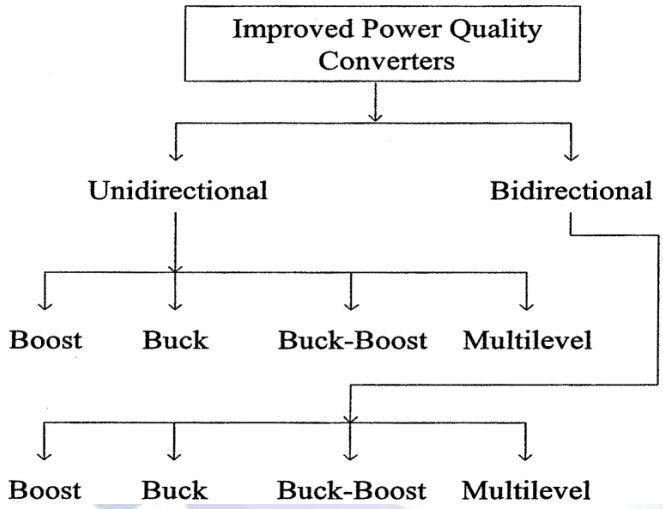
A. Operation of SEPIC converter

In positive and negative half cycle of the ac voltage the switches of upper and lower bridgeless converters are switched on and of alternatively. During the positive half cycle of ac input the upper buck boost converter operates in discontinuous conduction mode (DCM).During the negative half cycle the lower one operates in same way. In first half cycle the upper switch S_P on, energy stored in the inductor from the input and inductor current increases to its maximum value. Diode D_P completes the path of current flow in the input side. In the negative half cycle the upper switch S_P is turned off and the stored energy of inductor L_P is transferred to the outpur thus reducing inductor current from maximum to zero.

B. Operation of half bridge VSI

The controlled dc output voltage of the SEPIC converter is fed to the half bridge VSI for obtaining multiple output dc voltage scaling and high frequency isolation. The half bridge VSI is operated one switching cycle which is described in four states. In the first state, upper switch is turned on

and current circulates through the primary winding of high frequency transformer to the capacitor C_{12}. The second and fourth state are same and occur twice in each switching cycle. Diodes D_1, D_3, D_5, D_7, starts conducting and the inductor starts to store energy. Therefore the capacitors C_{01}, C_{02}, C_{03}, C_{04}, discharge through load and inductor current i_{L1}, i_{L2}, i_{L3}, i_{L4} increases. In second state, switches S_1 and S_2, and all the secondary diodes D_1-D_8 freewheels the stored energy until the voltage of HFT will become zero. Therefore inductor current i_{L1}, i_{L2}, i_{L3}, i_{L4} starts decreasing. In third state the second switch S2 is turned on and the input current flow through the upper capacitor C_{11} and the primary winding of the HFT. The diodes D_2, D_4, D_6, D_8 conducts in the secondary windings and inductor i_{L1}, i_{L2}, i_{L3}, i_{L4} starts storing energy. The same operating states repeat in each switching cycles.



IV. DESIGN OF PROPOSED SEPIC CONVERTER BASED MULTIPLE OUTPUT SMPS

To simulate the proposed bridgeless SEPIC converter based multiple output SMPS, it is essential to estimate components values.

TABLE-2 Parameters of Bridgeless converter Based Multiple Output SMPS

Components	Calculated	Selected	Experiment
Input inductor L_P and L_n	60µH	60µH	60 µH
Filter capacitor C_{in}	390nF	330nF	330 nF
Filter inductor L_{in}	3.07mH	2.5mF	2.5mF
Capacitor C_{11} and C_{12}	630µF	660µF	660µF

V. CONTROL OF PROPOSED BRIDGELESS CONVERTER BASED MULTIPLE OUTPUT SMPS

To control the SMPS it is carried out by using Neural network in place of PID controller due to which he settling time of boost output voltage power factor and efficiency is improved. And the half bridge VSI utilizes average voltage control.

A. Control of front end converter

According to the input ac mains voltage the control of the PFC bridgeless converter generates the PWM pulses for both switches (S_p and S_n). In this technique, the voltage voltge erroe V_e i.e. difference between the output dc voltage and the reference voltage V_{ref}.

$$V_e(n) = V_{ref} - V_{dc} \quad (1)$$

Where n represent the n^{th} sampling instant.

B. Control of Half bridge VSI

For controlling the output dc voltage of half bridge VSI an average current control scheme is used. The output voltage of highest rated winding output voltage V_{o1} i.e. 12volt is compared with the constant reverence voltage V_{o1ref}. The error voltage is fed to the neural network and its output is compared with the saw tooth signal to generate PWM switching signal to maintain output voltage constant. By controlling the impact of any individual output on over all variation in the duty ratio. If the load on any of the other winding is varied, according to the impact felt on the highest rated output the duty cycle under goes a change.

VI. EXPERIMENTAL RESULTS

A MATLAB prototype, whose parameters are listed in Table 2 has been constructed to evaluate the performance of the proposed scheme of **Figure 1.** Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

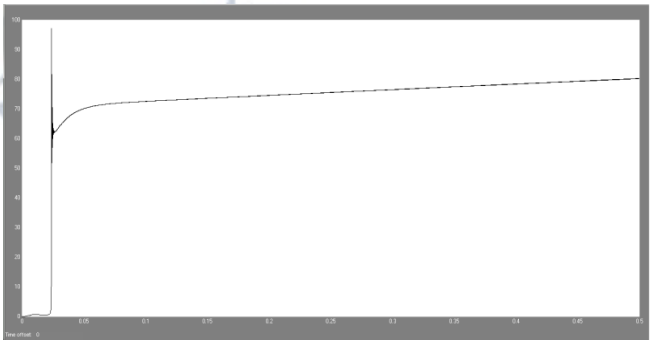


FIGURE 2-Efficiency of Multiple Output SMPS

VII. Conclusion

In this paper a single phase bridgeless SEPIC converter with low input current distortion and low conduction losses has been proposed and verified experimentally. Comparison is made in between the proposed SEPIC converter with neural network and conventional Buck-Boost converter with PID controller. The main feature of proposed method includes low voltage stress on semiconductor devices, high efficiency, low conduction losses, improved settling time and simplicity of design. The advantages are desirable features for high voltage and where the time of operation is very important matter. The measured efficiency was 80% in 5sec whereas in conventional method it was about 77% in 5sec. The proposed bridgeless converter PFC configuration , as describe in this paper, has been implemented to verify the performance of the system. The power factor of proposed is 0.95 and the conventional is 0.953. Finally, a prototype of the proposed bridgeless converter based multiple output SMPS has been developed to validate its performance experimentally. The proposed SMPS has shown satisfactory performance and hence can be extended easily to the other power conversion systems to satisfy the requirement of fast processor with high efficiency.

TABLE-3 Appendix

Parameter	Values
Nominal input AC mains voltage	260V , 50Hz
Half bridge VSI input voltages	310V
Multiple DC output voltages	12V, 5.5V, 3.3V, -12V

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