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Performance Analysis of Proposed Full Adder Cell at Submicron Technologies

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ABSTRACT

This paper presents an analysis of high-speed and low-voltage full adder circuit analysis. The proposed circuit analyzed for parameters like logic levels and power consumption. Full adder is an important circuit for designing many types of processors like microprocessors, digital signal processors, image processing and various VLSI applications etc. Many blocks of the designs, adders lie in critical data path of the circuit which affects the overall performance of the system. In this regards this paper analyses the proposed full adder cell at block level. Ripple carry adder is taken as the benchmark circuit to analyze the proposed full adder cell at 45nm technology.

KEYWORDS: *Full adder, Logic level, LP XOR gate*

I. INTRODUCTION

In processors adder is an important element. As such, extensive research continues to be focused on improving the power-delay performance of the adder. In VLSI implementations, parallel prefix adders are known to have the best performance. Fast and accurate operation of digital system depends on the performance of adders. Hence improving the performance of adder is the main area of research in system design. Arithmetic (such as addition, subtraction, multiplication and division) performed in a program, additions are required to increment the program counter and to calculate the effective address. show that in a prototypical RISC machine (DLX)72% of the instructions perform additions (or subtractions) in the data path. Over the last decade many different adder architectures were studied and proposed to speed up the binary additions.

From the past half century to the present date, we can find different types of full adder circuits in literature. In the early years of introduction to full adder circuits, tunnel diodes were used for the design of full adder circuits. Later Transistor Tunnel diodes became popular to design 1-bit full adder cell, and then came Diode-Transistor Logic (DTL). Afterwards MOSFET technology came to existence and design engineers started using the MOSFETs to design the circuits. Subsequently, full adder cell was designed with NOR/NAND gates and with Joseph son junctions. Over the time, the full adder cell has been designed in different ways with different logic styles. Since MOSFETs use in circuit design, engineers have been trying to reduce the power consumption and delay of a full adder circuit for the better performance of the system. The performance of the various full adder cells, in terms of the power and delay are compared in our previous paper [1].

Further this paper is organized as follows. Section II discusses about the analysis of the proposed full adder circuit at block level. The analysis is with respect to output logic level, number of transistors used to design the circuit and power dissipation of the circuit. Section III

gives the simulation environment and results. Conclusion has given in final section.

II. Analysis of the Proposed Full Adder circuit

Figure 1 represents the proposed 10 transistor full adder. Theory of the proposed full adder is described in [1] clearly. In this paper we tested whether the proposed cells work at block level or not. So a 16-bit ripple carry adder was designed and tested it to know the working of proposed full adder cells.

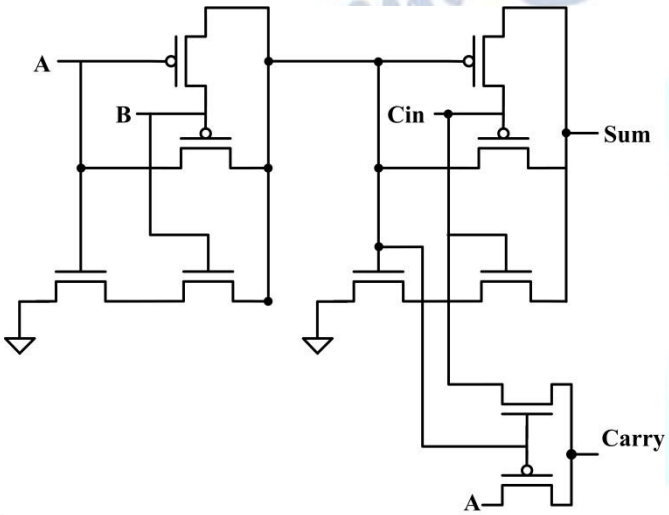

Figure 1: Proposed full adder circuit

Carry block of the proposed cell (Figure 1) used two pass transistors for carry signal generation. As the n-pass transistors have week 1 characteristics and strong 0 characteristics, p-pass transistor have strong 1 and week 0 characteristics the circuit cannot get rail to rail signal at the carry output section. So the proposed 10 transistor 1-bit full adder is modified to get the better results. That is, instead of pass transistors a transmission gate is used to obtain the carry signal so that a rail to rail logic was obtained. The modified proposed full adder cell is now a14 transistor cell and it is shown in Figure 2.

The figure of merit factors of a circuit design process is number of transistors, power dissipation, area, speed of the circuit and complexity. The proposed cell is designed with 10transistors only. In literature, there are full adder cells designed with less than ten transistors. Even though, the numbers of transistors are less compared to the proposed full adder cell, those circuits have degraded output levels. Those circuits have not produce rail to rail logic levels at output section.

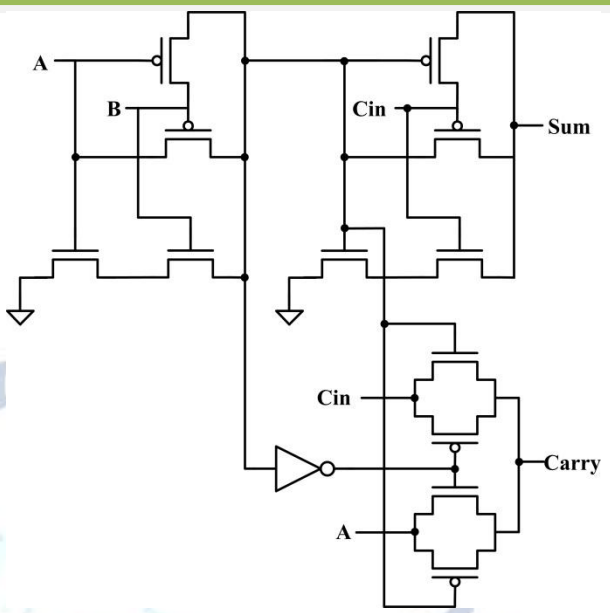

Figure 2: Modified Proposed full adder circuit

Table 1 gives the information of different types of full adders presented in this paper and also shows with which logic style each full adder is designed [1]. Most of the full adders in this work considered are which are designed with pass transistor logic. Based on the simulation results and wave forms obtained, it can be mentioned that the 6-T, 8-T, 10-T FA-I,10-T FA-II, full adder designed with GDI logic, and self-energy recovery full adder circuits give degraded carry out and sum signals at output.

Table 1: Features of Full adder designs under comparison

Full-Adder	# of Transi -stors	Circuit Type	Voltage Swing
6-T FA	6	PTL	Degraded
8-T	8	PTL	Degraded
10-T FA-I	10	PTL	Degraded
10-T FA-II	10	PTL	Degraded
GDI 10-T FA	10	GDI Logic	Degraded
14-T FA-I	14	PTL+TG	Full
14-T FA-II	14	PTL	Full
SERF	10	PTL	Degraded
Proposed 10-T FA	10	PTL	Threshold loss
Proposed 14-T FA	14	PTL+TG	Full

PTL - Pass Transistor LOGIC
TG - Transmission Gate Logic
GDI- Gate Diffusion Input

14-T FA-I, 14-T FA-II and the proposed fulladder

(with low Power XOR gate and pass transistors) give full swing at output node. While designing the proposed full adder circuit low power XOR gates are used. As per the paper [2],this low power XOR gate dissipates low power compared to other XOR gates considered in that paper.

III. Simulation Results

All designed circuits in this paper are simulated using Spectre simulator in Virtuoso Design Environment provided by Cadence Software. Designed circuits are captured using Generic Process Design Kit (GPDK) and 45nm technology transistor models are used. Simulations are done under GPDK45nm technology file provided by the Cadence Design Systems. The input combinations are taken from 000 to 111 and the simulation time is 20ns. The simulation results of the proposed circuits are shown in Figure 3 and 4.

To test whether the proposed adder will work for the multi bit addition or not, the modified full adder is used as the basic 1-bit full adder cell for 16-bit addition operation. This operation is performed between two 16-bit operands by using ripple carry adder architecture as shownin Figure 5, as benchmark circuit. Since adder cells are normally cascaded to form useful arithmetic circuits, their drivability must be ensured. In other words, the driving cell must provide not only full-swing voltage outputs but also sufficient current to the driven cell.

Figure 5 represents the 16-bit adder circuit, which is designed with ripple carry adder architecture. Figures 6 and 7 depict the two input operands A and B signals. Figure 8 represents the sum signals. The simulation waveforms prove that the designed 1-bit adder cell works for n-bit addition operations.

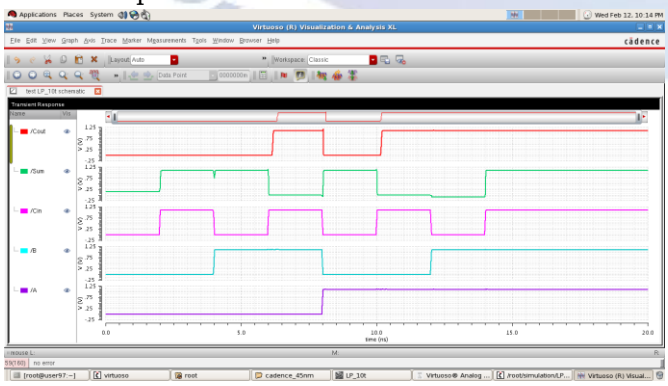

Figure 3: Simulation Results of the proposed 10T full adder

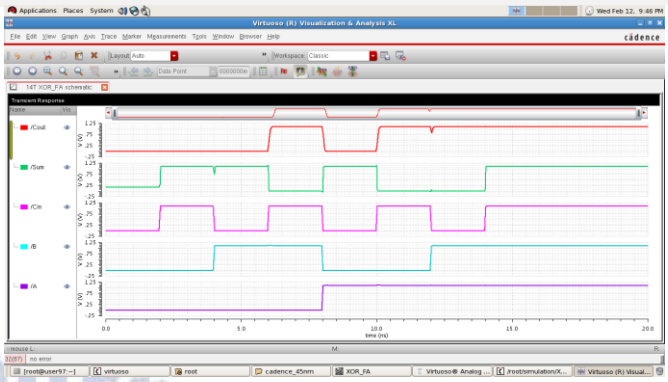

Figure 4: Simulation Results of the proposed 14T full adder

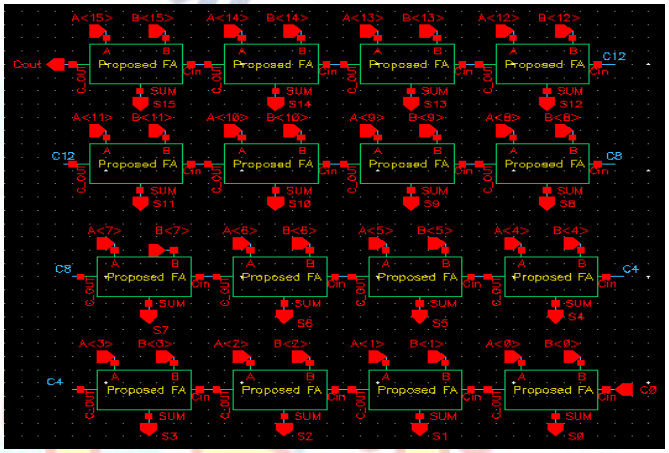

Figure 5: 16-bit addition operation using ripple carry adder

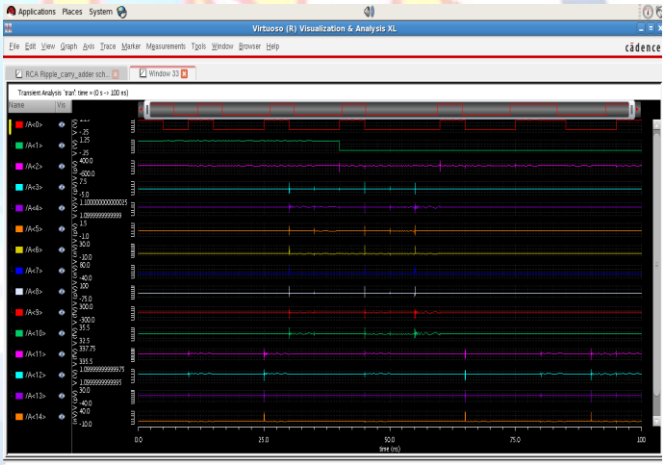

Figure 6: Simulation waveform of A input operand signals

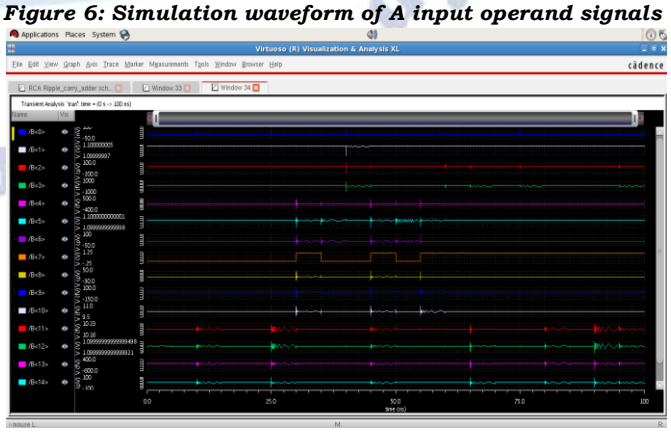

Figure 7: Simulation waveform of B input operand signals

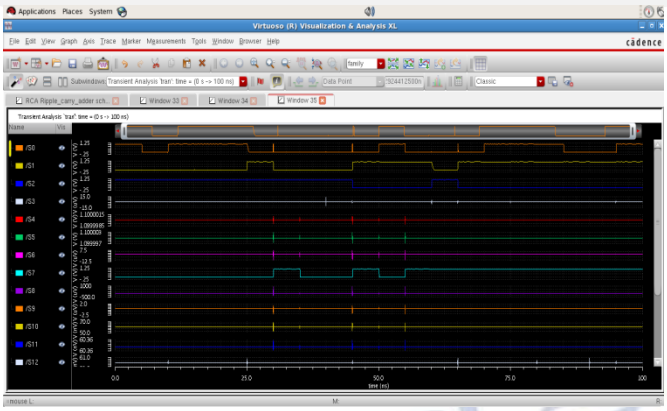

Figure 8: Simulation waveform of output sum signals

IV. Conclusion

In this paper, the proposed and modified full adder circuits are tested for the fitment of n-bit addition operation. The simulation results will prove that the proposed circuit will work for multi bit addition. All circuits are designed and simulated using cadence tools and the transistor models are taken from GPDK045nmtechnology files.

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