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Design of an Efficient Communication Protocol for 3d Interconnection Network

Shruthi.G[1] | Mohammad Khadir[2]

[1,2] Assistant Professor Department of Electronics and communication, Institute of Aeronautical Engineering, Hyderabad, Telangana, India

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ABSTRACT

Three-dimensional integrated circuits (3D ICs) provide better device integration, reduced signal delay and reduced interconnect power. They additionally give better layout flexibility by permitting heterogeneous integration, by taking the advantage of intrinsic capability of reducing the wire length in 3D ICs, 3D NOC Bus Hybrid mesh layout was suggested. This layout provides an apparently significant stage to implement economical multicast routings for 3D networks-on-chip. A unique multicast partitioning and routing strategy for the 3D NOC-Bus Hybrid mesh architectures to improve the system performance and to decrease the power consumption is being proposed. The planned design exploits the useful attribute of a single-hop (bus-based) interlayer communication of the 3D stacked mesh design to supply superior hardware multicast support. Finally customized partitioning approach and an effective routing method is given to decrease the average hop count and network latency. Compared to the recently designed 3D NOC architectures being capable of supporting hardware multicasting, huge simulations with traffic profiles reveals design exploitation, which is the planned multicast routing strategy will facilitate significant performance enhancements.

KEYWORDS: *NOC, Inter layer communication, 3d symmetric NOC, hybrid NOC BUS Architecture, Multicast*

I. INTRODUCTION

System on chip (SOC) is single integrated circuit, which consist of all other components required for an electronic system. In many system on chip applications a shared bus is required, this bus has to accept many requests. Be that as it may, such shared transport interconnection has some constraint in its versatility in light of the fact that just a single ace at any given moment can use the transport which implies all the transport gets to ought to be serialized by the mediator. Along these lines, in such a domain where the quantity of transport requesters is vast and their required data transmission for interconnection is more than the present transport, some other interconnection techniques to be considered.

The 2D symmetric NOC [1] design consists of 5X5 crossbar switch. The extension of 2D symmetric NOC's are 3D symmetric NOC, where it needs two additional ports resulting in 7x7 crossbar. The power consumption increased since number of ports were being increased. Hence power consumption is more compared to 2D symmetric NOC. 3D NOC-Bus Hybrid [2] mesh is being proposed to reduce the power consumption in 3D symmetric [5] NOC. It takes advantage of being short inter-layer distance around 20µm, which is characteristic feature of 3D ICs.

Table 1: difference between 2D and 3D IC'S

Metric	2D	3D
Total Area (mm2)	31.36	23.4
Total Wire Length(m)	19.107	8.238
Max Speed(Mhz)	63.7	79.4
Power @ 63.7Mhz(mW)	340.0	324.9
FFT Logic Energy(uj)	3.552	3.366

Network on Chip (NOC) could be a new paradigm for System on Chip [2] (SOC) style. Increasing integration produces a state of affairs wherever bus structure that is usually employed in SOC becomes blocked and raised capacitance poses physical issues. In NOC [3] ancient bus structure is replaced with a network that could be a heap just like the web. Information communications between segments of chip area unit packetized and transferred through the network. The network consists of wires and routers. Processors, recollections and alternative IP-blocks (Intellectual Property) area unit connected to routers. A routing formula plays a big role on network's operation. Routers create the routing choices supported the routing formula.

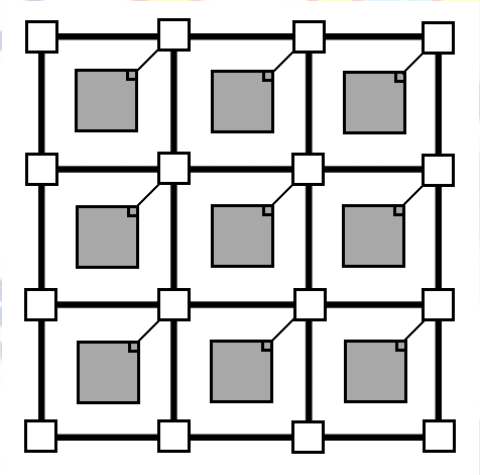

Figure 1: Network on Chip

The network traffic in Network on Chip is split to two varieties, guaranteed Throughput (GT) and Best Effort (BE) traffic. Guaranteed throughput is additionally typically known as guaranteed Service (GS). GT traffic guarantees that some portion – for instance, ninety-nine present of information overtakes the receiver in it a slow slot. GT provider assumes that the sender complies with networks operation necessities. Secure outturn works best with routing algorithmic rule that acts like circuit switched network. Best-effort packets are arbitrated as trustworthy as attainable. Still, there are not any guarantees that BE packets can ever reach the receiver. Latencies will vary and within the worst case packets may be lost. Traffic in a very basic packet switched network.

Chip design has distinct aspects. As process power has accrued and data-intensive applications have emerged, the challenge of the communication side in single-chip systems, Systems-on-Chip (SOC), has attracted increasing attention. This survey treats a distinguished idea for communication in SOC called Network-on-Chip (NOC). As can become clear within the following, NOC doesn't represent a certain new various for intra chip communication [4], however, is quite a plan that presents a unification of on-chip communication solutions.

II. LITERATURE SURVEY

At one corner of the architectural space outlined is the Pleiades architecture [Zhang et al. 2000] and its instantiation, the Maia processor. A microprocessor is combined with a relatively fine-grained heterogeneous collection of ALUs, memories, FPGAs, etc. An interconnection network allows arbitrary communication between modules of the system. The network is hierarchical and employs clustering in order to provide the required communication flexibility while maintaining good energy-efficiency.

At the opposite corner are a number of works, implementing homogeneous coarse-grained multiprocessors. In Smart Memories [Mai et al. 2000], a hierarchical network is used with physical clustering of four processors. The flexibility of the local cluster network is used as a means for re-configurability, and the effectiveness of the plat-form is demonstrated by mimicking two machines on far ends of the architectural spectrum, the Imagine streaming processor and Hydra multiprocessor, with modest performance degradation.

The global NOC is not described, however. In the RAW architecture [Taylor et al. 2002], on the other hand, the NOC which interconnects the processor tiles is described in detail. It consists of a static network, in which the communication is preprogrammed cycle-by-cycle, and a dynamic network. The reason for implementing two physically separate networks is to accommodate different types of traffic in general purpose system. The Eclipse [Forsell 2002] is another similarly distributed multiprocessor architecture in which the interconnection network plays an important role. Here, the NOC is a key element in supporting a sophisticated parallel programming model.

III. RELATED WORK

A. Protocol

The protocol issues the strategy of flow of data through NOC. Switching is defined as data flow while routing as path behind the flow, which is in agreement with Culler et al. [1998].Circuit switching involves set up from beginning to end until data transfer is complete whereas Packet switching is transferred on the per-hop basis, each packet containing routing information.

B. Packet Format

During multicast routing, messages received by destination node will check the address in message header with primary destination node. If matched, the messages are copied and sent in conjunction with neighboring node header in accordance to routing algorithm which is being proposed. 3D NOC Hybrid mesh design is crossing of two completely different communication media, it would associate with a custom packet format to support multicasting. The packet format is based mostly on multicasting packet format in Hamiltonian model. The packet consists of a header flit and a number of payload flits whereas every flit is p bits wide. The primary bit in flits is reserved for bop (begin-of-packet) flag and the second bit for the EOP (end-of-packet) and s bits are reserved for routing information (RI). The remaining bits are allocated for higher level protocols (HLP). The RI field is having four fields Routing Mode (RM), Communication Mode (CM), Number of Destinations on the Bus (NDB), and Destination Address (es) (DA).

The RM bit indicates whether or not the routing mode is unicast or multicast ('0'/'1'). The CM bit defines whether or not the communication mode is intra layer or layer ('0'/'1') in multicast routing. If the mode is intra layer, then it implies that this target destination node is found within the same layer (no layer communication is needed) where first DA field (DA0) is used simply. Else the current target destination node(s) are situated within layer(s) other than the current layer. There is a possibility that more than one destination node is connected to same bus in case of interlayer multicast mode (RM=CM='1'). The NDB field is employed for such cases to point the quantity of destination nodes on the bus. During this format, the maximum number of supported destination nodes on a bus is 2r. Each DA field is split into two subfields, layer and layer Id (LID) based on labelling and partitioning technique which uniquely specify each node position.

ALGORITHEM TWO-PHASE FOR 3D MULTICAST PARTITIONING

Input: (L, K, S, D) – {L: Number of layers, K: Number of nodes per layer, S: Source node, D: Destination set}

Output: (DL , DU) – {DL and DU : Destination set in low-channel and high-channel subnetwork, respectively}

```
1:  for i = 0 →L−1     do
2:      for j = 0 → K − 1 do
3:          if Label (Di (j)) < Label(S) then
4:              Add Di (j) to DU;
5:          else
6:              Add Di (j) to DL ;
7:          end if
8:      end for
9:  end for
```

10: Sort DU in increasing order according to the label numbers. If some nodes have same label, sort them locally in increasing order using layer numbers (the node with the same layer ID as the source node comes first);

11: Sort DL in decreasing order according to the label numbers. If some nodes have same label, sort them locally in decreasing order using layer numbers (the node with the same layer ID as the source node comes first);

12: Construct two messages for two disjoint sub networks using DU, and DL in their headers.

C. Multicast Routing Algorithm

The multicast routing of packets that takes place within 3D NOC-Bus Hybrid mesh design that relies on Two-Phase 3D Multicast Routing algorithm. The direction of data packet that needs to be traversed, depends on current node location (Node C), the location of current target destination node (Node D), eastern neighboring node location (Node Eastern Neighbor), western neighboring node location (Node Western Neighbor) as well as current X-coordinate (X Node C) and current target distinction (X Node D) nodes. Whenever a router sends a multicast packet to its up/down port, bus design have multicasting support which is required to deliver the packet to connected destination node(s) of router(s). Utilization of the bus design projected, which offered multicast protocol that used for packet based transactions is been used. Hamiltonian path based static routing algorithm

which is being proposed is tailor-made for 3D NOC-Bus Hybrid mesh design. It's a deadlock-free path model.

ALGORITHM FOR 3D MULTICAST ROUTING

Input: NodeC, NodeD, XNodeC, XNodeD, NodeEastern
Neighbor, NodeWestern Neighbor

Output: Next Hop (East, West, North, South, Local, Up/Down)

1: if Label (NodeC) = Label (NodeD) then
2: if Layer ID (NodeC) = Label ID (NodeD) then
3: Deliver the packet to the Local node and exit;
4: else
5: Send the packet to the Up/Down output port (connected bus) towards the destination(s);
6: end if
7: else if Label (NodeC) < Label (NodeD) then
8: if XNodeC < XNodeD then
9: if Label (NodeC) < Label (NodeEastern Neighbor) then
10: Send the packet to the East output port towards the destination(s);
11: else
12: Send the packet to the North output port towards the destination(s);
13: end if
14: else if XNodeC > XNodeD then
15: if Label (NodeC) < Label (NodeWestern Neighbor) then
16: Send the packet to the West output port towards the destination(s);
17: else
18: Send the packet to the North output port towards the destination(s);
19: end if
20: else
21: Send the packet to the North output port towards the destination(s);
22: end if
23: else
24: if XNodeC < XNodeD then
25: if Label (NodeC) > Label (NodeEastern Neighbor) then
26: Send the packet to the East output port towards the destination(s);
27: else
28: Send the packet to the South output port towards the destination(s);
29: end if
30: else if XNodeC > XNodeD then
31: if Label (NodeC) > Label (Node Western Neighbor) then
32 Send the packet to the West output port towards the destination(s);
33: else
34: Send the packet to the South output port towards the destination(s);
35: end if
36: else
37: Send the packet to the South output port towards the destination(s);
38: end if
39: end if

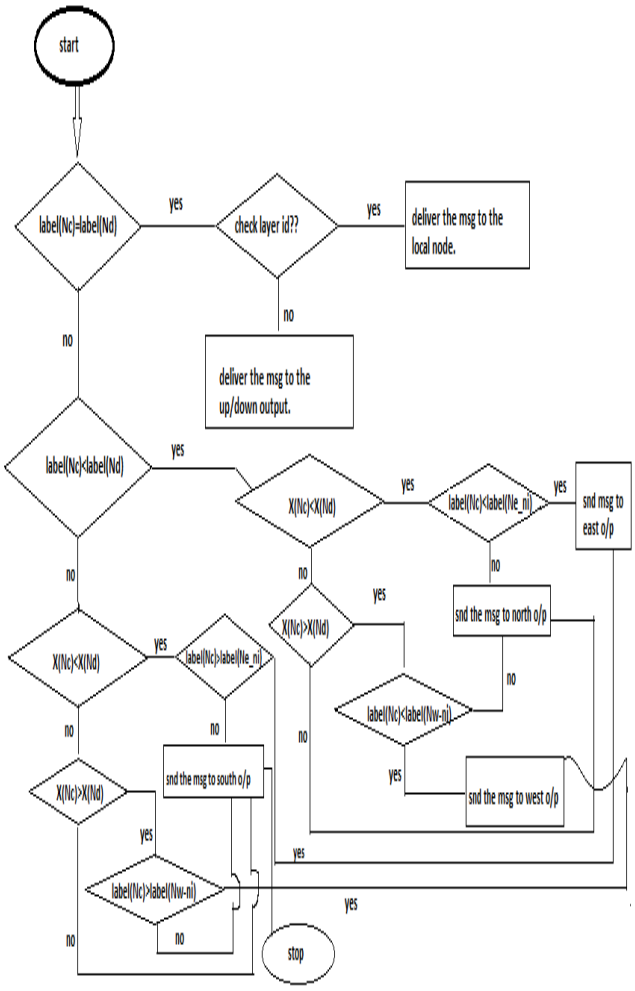

Figure No. 2: FLOW CHART FOR 3D MULTICAST ROUTING

IV. SIMULATION RESULTS

Average network packet latency and an accurate NOC simulation domain cycle is being performed in VHDL which is used to determine the efficiency of 3D Hybrid NOC Bus. Conventional two-phase partitioning and Hamiltonian path based routing is being used in symmetric 3D-NOC bus. 3D NOC-Bus Hybrid proposed multicast partitioning

and routing methods are used to analyze synthetic and realistic traffic patterns. In symmetric 3d-mesh NOC architecture, the routers have 7-ports, and for 3D Hybrid NOC-Bus routers have 6 input/output ports. Switch allocator is based on the round robin mechanism in both methods used.

To perform the simulations, a mix of unicast (80%) and multicast (20%) traffic was used. For the unicast portion of the traffic, uniform, hotspot 10 percent, and Negative Exponential Distribution (NED) traffic patterns are being used. Within the uniform traffic pattern, a node sends a packet to different nodes with an equal chance. Within the hotspot traffic pattern, messages are destined to a specific node with a particular (10% beyond average) chance and are otherwise uniformly distributed. The NED may be traffic model supported Negative Exponential Distribution wherever the probability that a node sends a packet to a different node exponentially decreases with the hop distance between the 2 cores. This synthetic traffic profile accurately captures key applied mathematics behavior of realistic traces of communication among the nodes, to come up with the multicast portion of the traffic, we tend to use the uniform distribution given sure making ready the destination set of every multicast message. We tend to use a 48-node (three layers of 4×4 mesh) network and assumed that the buffer size of every FIFO was eight flits, and data width was set to 64 bits.

4.1 SIMULATION RESULTS FOR 3D SYMMETRIC NOC:

In 3D symmetric NOC the number of destination nodes is being set to six, with length of seven-flits the packet length is being set and used in first experiment set. The average packet latency (APL) curves for uniform-uniform (i.e. 80% uniform-unicast and 20% uniform-multicast), hotspot 10% uniform and NED-uniform traffic patterns with varying average packet arrival rates (APAR). For the hotspot 10% traffic pattern, the nodes at (2, 2, 2), (2, 3, 2), (3, 2, 2), (3, 3, 2) are destined as the hotspot nodes. It can be observed for all the traffic patterns, that the network using proposed Hamiltonian path based multicasting saturates at higher injection rates. Improvement in the max packet delay for the multicast massages by reducing the Hamiltonian path lengths and utilizing the broadcast and high-speed characteristics of vertical buses is being achieved.

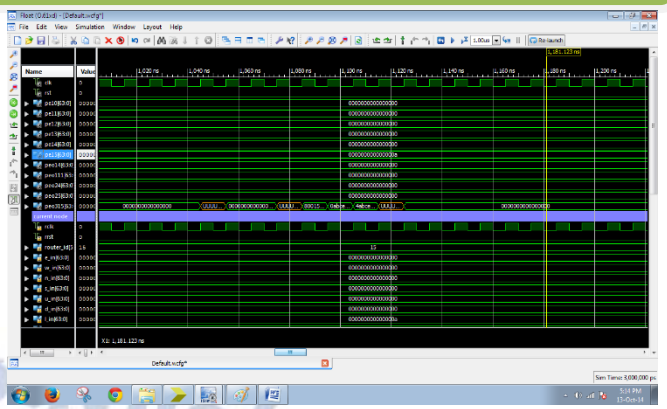

Figure No 3: Showing the data received at the destination node.

Device utilization summary:

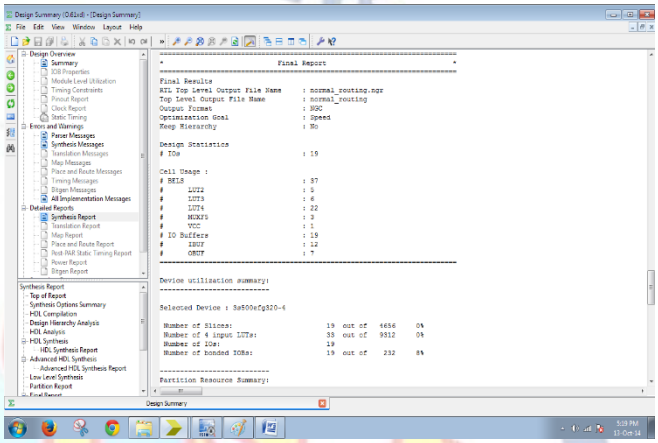

Figure No 4: Showing the devise utilization report for symmetric NOC Architecture

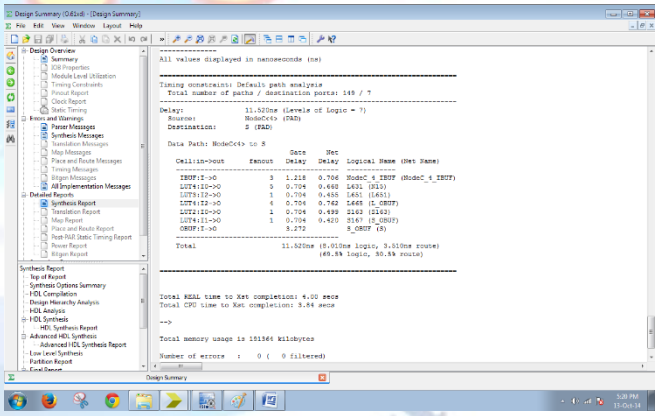

Figure No 5: Showing the timing report for symmetric NOC Architecture

4.2 SIMULATION RESULTS FOR 3D HYBRID NOC:

We modified NOC parameters used in first set in the second experiment set. The destination node number is set to 12 and ten-flit packet length is been used for simulations. The packet latency for uniform-uniform, hotspot 10%-uniform and NED-uniform traffic patterns with varying APAR. Improved average packet latency for varying average packet arrival rates in contrast to symmetric 3D-mesh NOC has been revealed in this experimental set.

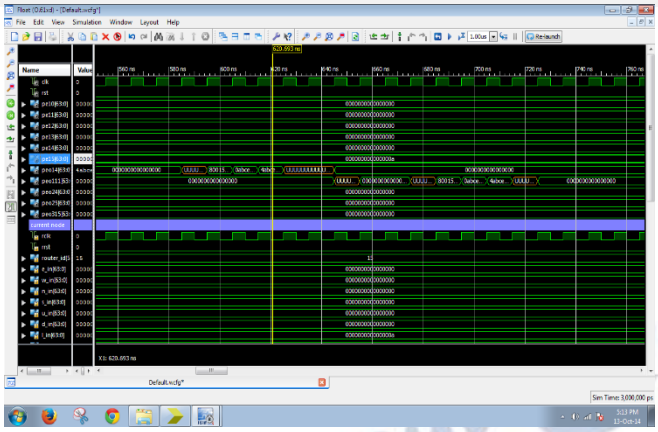

Figure No 6: Showing the data received at the destination node.

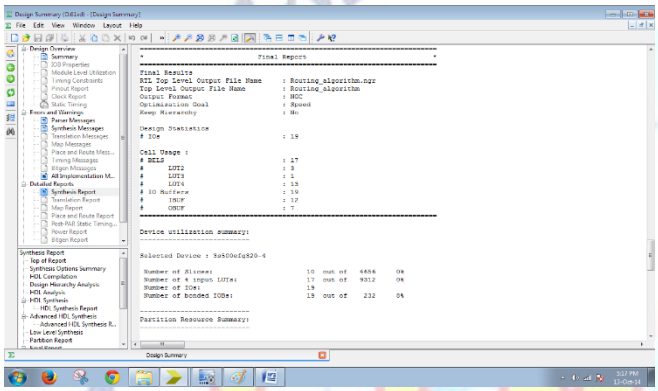

Figure No 7: Showing the devise utilization report for hybrid NOC Architecture

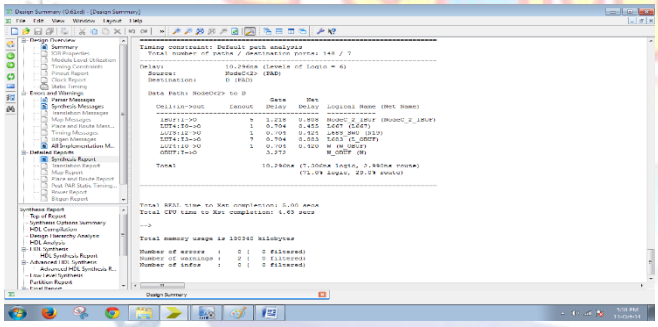

Figure No 8: Showing the timing report for Hybrid NOC Architecture

V. CONCLUSION

In this paper, an efficient multicast partitions and routing strategy for the 3D NOC-Bus Hybrid mesh architecture was proposed to support multicasting, thereby improving the overall NOC performance. The proposed architecture exploits the beneficial attribute of a single-hop (bus-based) interlayer communication of the 3D stacked mesh architecture to provide high-performance hardware multicast support. To this end, we proposed a customized labeling and partitioning method to efficiently split the network into well-balanced subnet works and enhances the multicast routing function. In addition, we presented a Hamiltonian path based multicast routing algorithm which exhibits a high degree of parallelism and reduces the startup latency by generating only two messages for created subnetworks.

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