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Design of CMOS Based PLC Receiver

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ABSTRACT

This paper presents a power line communications (PLC) receiver in ICs. The PLC is one in which the power pins and the power distribution networks of ICs are used for data communication as well as power delivery. PLC is used in order to reduce the number of input pins that an IC needs to couple the test data signals to each and every node. The main design objective of the proposed Low Voltage CMOS Schmitt trigger for PLC receiver is the power efficient operation, since power is one of the most important criterions in the VLSI design. Schmitt trigger circuits are widely used for waveform shaping under noisy conditions in electronic circuits. The hysteresis in a Schmitt trigger offers better noise margin and noise stable operation. In this paper, we report novel Schmitt trigger circuit designs in CMOS for operation at 1V and below using a dynamic body-bias method. The PLC receiver designed in 0.18µm CMOS technology under a supply voltage of 1V with the help of Tanner EDA tool, to achieve extreme low power consumption. It is found that the power consumption of this new PLC receiver is only 0.769mW, which is very less than presently existing designs.

Keywords *— PLC Receiver, Power line communications, CMOS, Power consumption.*

I. INTRODUCTION

Today's VLSI technology is advancing in such a way that the designers can incorporate a large number of functions inside a chip. Microprocessors are one of the best examples for this. Day by day the size of ICs reduces and the operations it can perform are increasing. So many challenges still exist such as, the need of proper provision for the thermally generated heat removal, the number of the input output pins that an IC needs, proper power supply injection etc., due to which there exists limits on incorporating functions inside ICs. Also routing inside the IC too has a major role in it. There should also be the provisions in ICs like sensors to detect what is happening inside each and every point and if anything happens wrongly, the normal state have to be recovered. Even though the increase in system complexity is an advantage in the sense that the size of ICs can be reduced, with that there should be new inventions for proper data passage inside the same. The power line communication aspect presented in this paper is one of such methods.

In power line communication, it efficiently uses the power distribution networks inside ICs since they are the only components that reach each and every node. So if there have a provision to pass the test data, which are used for fault diagnosis, scan design etc. to whichever areas we need to apply the test that will be an attractive way of communication in ICs, So that the routing overhead inside the ICs to pass these testing data can be intelligently avoided. So in PLC, the power distribution networks are used for power delivery and also data communication. The test data are superimposed on the power signal and are transmitted through the power distribution networks of ICs rather than the separately allotted

routing paths. Also the number of power pins can be reduced since there is no need to carry the test data through the input pins. Of course, adopting such a power line communication always has to overcome the extreme noise level at the power lines. So there should be effective methods to overcome the same. Essentially there is the need of receivers at each and every node to extract these data signals efficiently from the power lines. Many variants of the same already exist, but a power efficient design is not yet met. Why the receiver should be power efficient is because, otherwise if each unit of receiver consumes such huge power, the overall power consumption of the entire chip will increase by a large value, which is hard to afford.

In this paper, such a proposed Low Voltage CMOS Schmitt trigger for PLC receiver is designed in 0.18μm CMOS technology under the supply voltage of 1V. The methods that are incorporated to achieve the power reduction are very simple to understand and realize.

II. PREVIOUS WORKS

In PLC area, previous works are already conducted to reduce the ICs smaller by incorporating the PLC to reduce the pin count, area and hence the cost of the chip. So many such works at the base levels are already carried out in this area. Works are conducted in ICs to measure the data propagation loss from the main power supply to the internal nodes and also, communication technologies are put forward such as the Ultra Wide Band (UWB) and Direct Sequence Code Division Multiple Access (DS CDMA) for successful test data passage inside ICs with reduced noise level.

Since our work concentrates on the design of the PLC receiver let's have a brief literature review on the same.

At first, a data recovery block was designed which can extract the test data signals from the power line modulated with impulses in which Ultra Wide Band communication technology was adopted. The sensing scheme inside the recovery block was designed in such a way that it maintains very small Power Supply Rejection Ratio(PSRR) and it is found that the data recovery block was able to extract the data with about the amplitude of 90mV and with the period of 300pS. The design was implemented in TSMC 0.18µm CMOS technology which had a power consumption of 2.8mW.

Later, a work on the power distribution networks of microprocessors is carried out by using the UWB communication technology for test data transmission by superimposing UWB impulses on the power lines. Based on the resultant characteristics of the PDNs, a data recovery block design was proposed and the work was implemented in TSMC 0.18µm CMOS technology under a supply voltage of 1.8 V with a pulse repetition rate of 200MHz and the resultant power consumption was at about 4.42mW.

A robust receiver for PLC was proposed in ICs which employs the differential Schmitt trigger as the third stage of the receiver for better noise immunity and also to tolerate supply voltage variations and drops. Thus the aim was on the robustness and the design was proposed in 0.18µm CMOS technology under a supply voltage of 1.8 V. The measurement results showed that the receiver can tolerate up to 22.2% of the supply voltage drop under the signal-to-noise ratio (SNR) of 16.3 dB. The power consumption was 2.4mW.

A PLC receiver was designed in 0.18µm CMOS technology under a supply voltage of 1.8 V, which can be applicable to fault diagnosis, scan design, system debugging like low data rate communications. The receiver was designed with three building blocks, the level shifter, signal extractor, and the logic restorer. The main aim of this work was not the high data rate communication, but the robust operation under variations of supply voltage and droops. Amplitude Shift Keying (ASK) approach was put forward for the superimposition of the test data signals with the power lines. Adopting binary ASK has the advantage of less circuit complexity, simple and easy implementation and hence lower cost and area. But the main problem was on the ability to withstand the noise level that is present in the test data which couples through the power lines. To overcome the same, differential concepts are intelligently employed in the receiver which could achieve high level of noise rejection. Differential Schmitt trigger was the key building block in this design, since it was the major contributor for the noise immunity. The measurement results showed that the receiver can tolerate a voltage drop of up to 0.423 V, which has a power dissipation of 3.26mW and a core area of 74.9µm × 72.2µm.

So in this paper, a proposed Low Voltage CMOS Schmitt trigger for PLC receiver is designed to extract the test data signals superimposed on the power lines. The main aim was the power efficient operation since power is one of the most important criterions in the VLSI design. Also in the PLC, we not only need one or two of these receivers, but needs it in places wherever necessary or most probably at each and every nodes of the ICs. So, if each unit consumes large power, the total power consumption of the entire IC will increase dramatically which is not affordable, and should mind that these receivers are used only for extracting the test data signals from the power lines and there will be so many other components inside the same IC for other operations. So power efficient design has its own importance in present VLSI design with increased complexity especially in microprocessor like ICs. This paper presents the design of proposed Low Voltage CMOS Schmitt trigger for PLC receiver in 0.18-μm CMOS technology under the supply voltage of 1V with the help of Tanner EDA tool.

III. PROPOSED LOW VOLTAGE CMOS SCHMITT TRIGGER FOR PLC RECEIVER

The Proposed Low Voltage CMOS Schmitt Trigger for PLC receiver designed in this paper under a supply voltage of 1V in CMOS 0.18-μm technology using Tanner EDA tool which consists three major building blocks, they are the level shifter, the signal extractor and the logic restorer. The block diagram of the Proposed Low Voltage CMOS Schmitt Trigger for PLC receiver is shown in fig.1. The test data is represented by Vdd(t) and the main power signal by VDD. So VDD+Vdd(t) represents the test data superimposed on the power lines. The input signal is the power line signal in which the test data is superimposed and it is supplied to each of the building blocks. The output of the level shifter is the input of the signal extractor and the output of it, which is a differential signal and is applied to the logic restorer. The detailed operation and design concepts of each of the building blocks are described below.

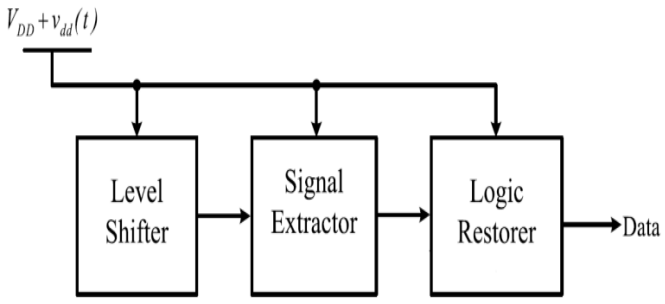

Fig.1 Proposed Low Voltage CMOS Schmitt Trigger for PLC Receiver

1. Level Shifter

The level shifter is the first stage in the proposed PLC receiver which is nothing but a common source amplifier having diode connected load and is shown in fig. 2. The purpose of this level shifter is to lower the DC level of the signal at the output so that, it will be easy for the subsequent blocks to process the data. Also since the test data signals are superimposed on the power lines, this stage should have the ability to sense the variations that are present in the power lines and for that, its sensitivity to the input signal is purposefully lowered and the same to power signal is increased by lowering the characteristic called the Power Supply Rejection Ratio (PSRR). It can be expressed as in equation (1)

$$PSRR = Av/Avdd \quad (1)$$

Where Av is the small signal voltage gain of the circuit and $Avdd$ is the small signal voltage gain from the power input to circuit's output. The small signal voltage gain can be expressed in terms of gm as

$$Av = -\ gm1/gm2 \quad (2)$$

The small signal voltage gain from the supply voltage can be expressed as

$$Avdd = \frac{r01}{(1/gm2)+r01} = 1 \quad (3)$$

Substituting (2) and (3) in (1) gives

$$PSRR = -\ gm1/gm2 \quad (4)$$

PSRR can be again represented in terms of device dimensions and overdrive voltage as

$$PSRR = \frac{\mu n \left(\frac{W}{L}\right)1 (Vgs-Vth)1}{\mu p \left(\frac{W}{L}\right)2 (Vgs-Vth)2} \quad (5)$$

Since we need a level shifter having a low PSRR, the equation (5) can be treated in two different ways. In order to reduce the PSRR, either we can reduce the device dimension of transistor M1 and can increase the same of M2. Also the overdrive voltage of M1 should be lowered and that of M2 should be made high compared to M1. These two

concerns should be kept in mind while designing the level shifter stage for a smaller PSRR.

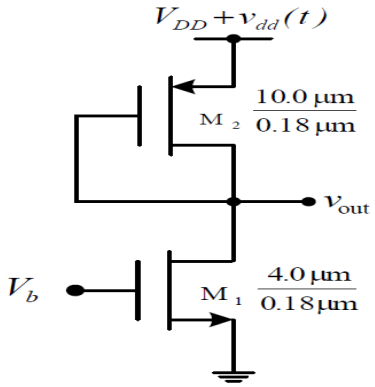

Fig. 2 Level Shifter

2. Signal Extractor

The signal extractor in the proposed design is a differential amplifier and is shown in Fig 3. The output of the level shifter is simultaneously fed to two input terminals of the differential amplifier, out of which a low pass filter is connected to one of the terminals. The low pass filter is used in this design to extract the DC value from the level shifter output. Since the differential amplifier has a property of rejecting the common mode signal, which is the DC signal in our design, is thus successfully eliminated. The use of the same has another advantage that it reduces the noise levels that are already present in the signals. The signal extractor of the proposed design is shown in fig. 3.

The signal extractor converts the single ended output of the level shifter to a differential signal. In this proposed design we consider only signal output. This output is connected to the next block new logic restorer.

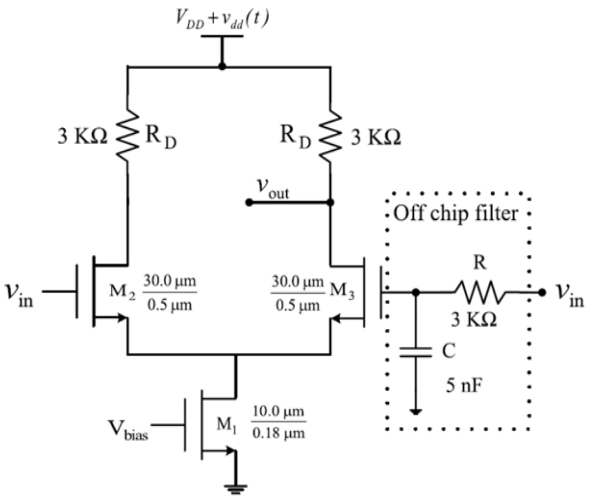

Fig. 3 Signal Extractor with Low Pass Filter

3. Logic Restorer

The logic restorer is the block which contributes to a great part in the noise immunity of the entire system. It is a Low Voltage CMOS Schmitt Trigger with tunable hysteresis property. The main advantage of using this Schmitt trigger is that, it is excellent in handling the situations of extreme noise and disturbances. The Low Voltage CMOS Schmitt trigger based logic restore employed in the design is shown in fig. 4.

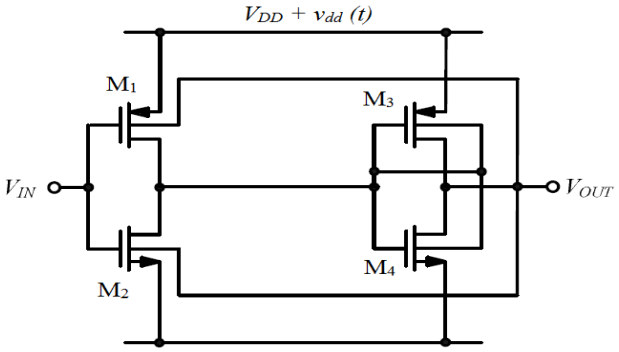

Fig. 4 Low voltage CMOS Schmitt Trigger based logic restorer

Schmitt trigger circuits are widely used for waveform shaping under noisy conditions in electronic circuits. In VLSI circuits, they are often used at the chip input side and as single-ended receivers in DRAMs. The hysteresis in a Schmitt trigger offers better noise margin and noise stable operation. With proliferation of portable devices, low power circuits are extremely desirable. In a recent work, a low power Schmitt trigger circuit design is reported for 3V operation. The cascade architecture used in this design limits lowering the operating voltage. In this paper, we report novel Schmitt trigger circuit designs in CMOS for operation at 1V and below using a dynamic body-bias method.

IV. MEASUREMENT RESULTS OF PROPOSED LOW VOLTAGE CMOS SCHMITT TRIGGER FOR PLC RECEIVER

1. Level Shifter

The level shifter that is the common source amplifier with diode connected load is simulated with the proper bias voltage at the gates of the transistor M2.The schematic diagram of the level shifter is designed with the help of Tanner tool and is shown in fig. 5. The timing response obtained is shown below in fig. 6.

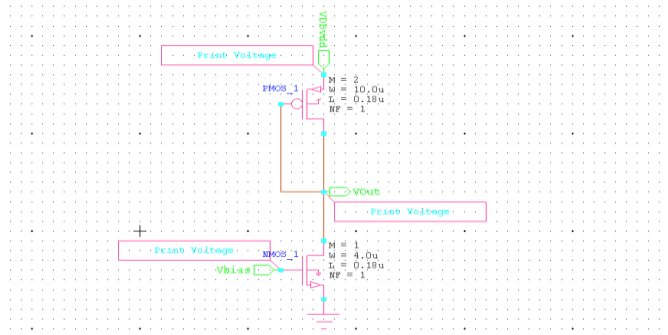

Fig.5 schematic diagram of the level shifter

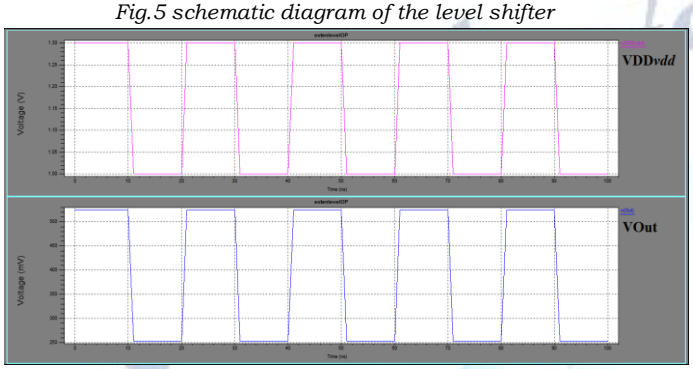

Fig. 6 Level Shifter Transient Response

Fig. 5 shows the input and output voltage waveforms of the level shifter for the data rate of 100 Mb/s. The supply voltage is 1.3V with the superposition of the data signal. The top waveform is the input signal superimposed on the supply voltage, in which the voltage level of 1.3V represents logic 1 and 1V represents logic 0. The bottom waveform shows the output signal of the level shifter, in which the voltage for logic 0 or the baseline voltage of the signal is shifted down to 250mV and that for logic 1 down to 525mV.

Average power consumed for level shifter is 0.6497022439e-3 (m Watts).

The layout of the level shifter is shown in fig. 7

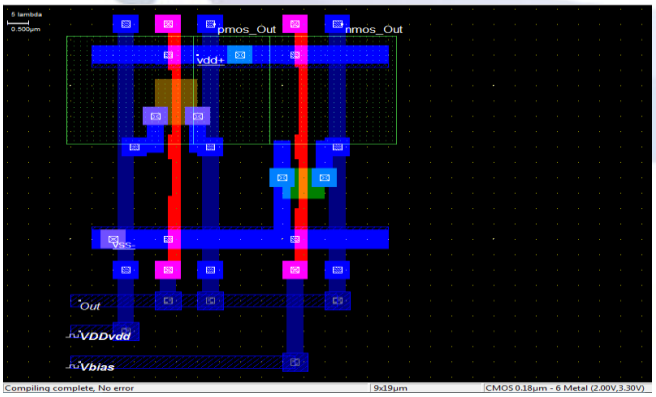

Fig. 7 Level Shifter Layout

2. Signal Extractor

The signal extractor is a differential amplifier, in which one input is connected to an *RC* low-pass filter. The schematic diagram of the signal extractor is designed with the help of Tanner tool and is shown in Fig. 8 and Fig. 9 shows the input and output voltage waveforms of the signal extractor.

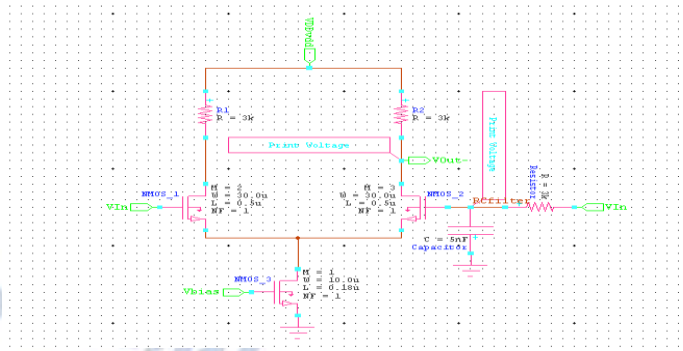

Fig. 8 schematic diagram of the signal extractor

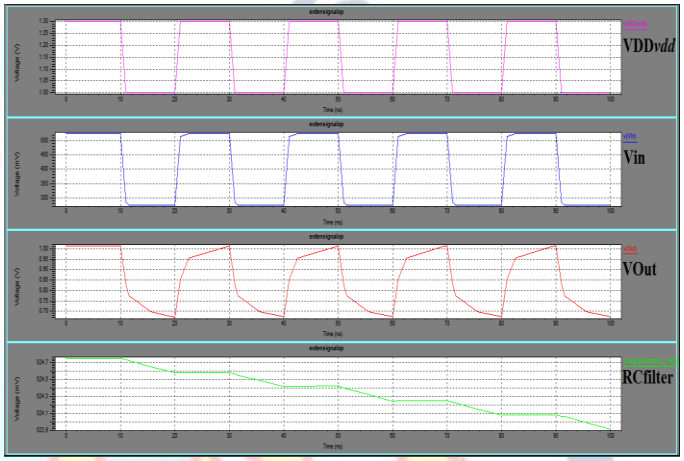

Fig. 9 Signal Extractor Transient Response

The top waveform is the input signal superimposed on the supply voltage. The second waveform is the applied input signal whose baseline voltage, or the voltage for logic 0, is set to 250mV and the voltage for logic 1 to 525mV. The third waveform shows the output voltage, which varies between 0.70mV and 1.1mV. The bottom one shows the output voltage of the *RC* low-pass filter, which varies between 523.9mV and 524.7mV.

Average power consumed for signal extractor is 0.767687446e-03 (m Watts).

The layout of the signal extractor is shown in fig. 10

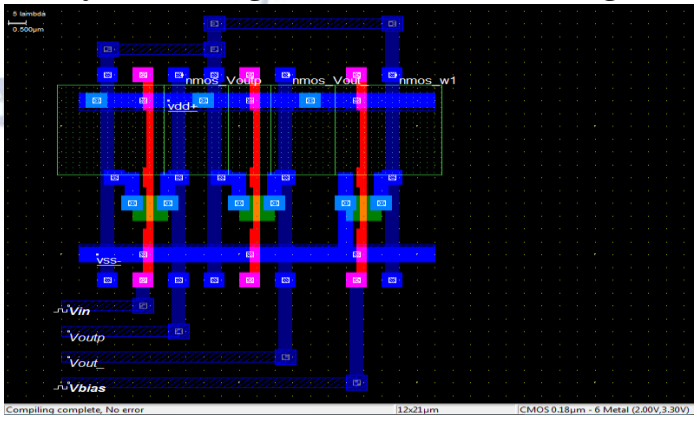

Fig. 10 Signal Extractor Layout

3. Logic Restorer

Low Voltage CMOS Schmitt trigger based Logic restorer is proposed for PLC receiver. The schematic diagram of the logic restorer is designed with the help of Tanner tool and is shown in Fig. 11. The outputs of the differential amplifier are supplied to the inputs of the logic restorer. The simulation results of the logic restorer are shown in fig. 12

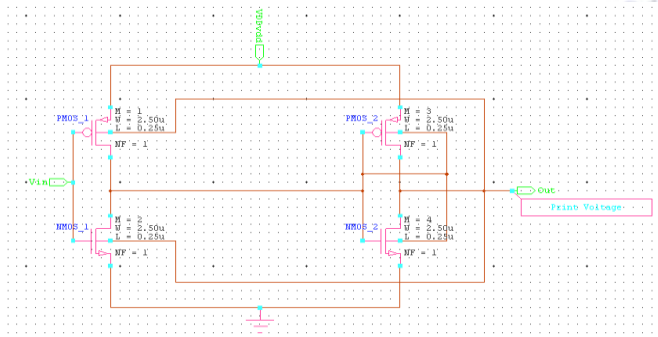

Fig. 11 schematic diagram of the logic restorer

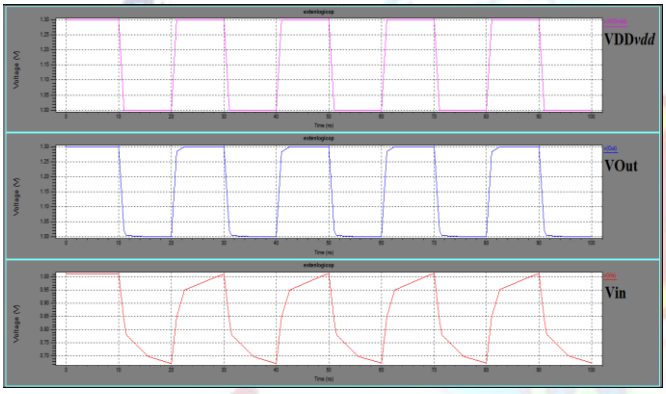

Fig. 12 Logic Restorer Transient Response

Fig. 12 shows the input and output voltage waveforms of the logic restorer. The top waveform is the input signal superimposed on the supply voltage. The second waveform shows the restoration of the logic values. The bottom waveforms show the applied input signal.

Average power consumed for logic restorer is 0.7690421771e-03 (m Watts).

The layout of the logic restorer is shown in fig. 13

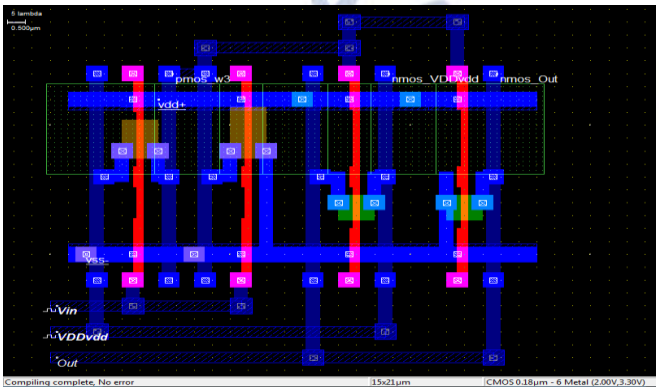

Fig. 13 Logic Restorer Layout

4. Proposed PLC Receiver

Now, the three blocks of the PLC receiver are connected together after the verification of the operation of individual blocks. The schematic diagram of the Proposed Low Voltage CMOS Schmitt Trigger for PLC Receiver is designed with the help of Tanner tool and is shown in Fig. 14 and Fig. 15 shows the input and output voltage waveforms of the PLC receiver.

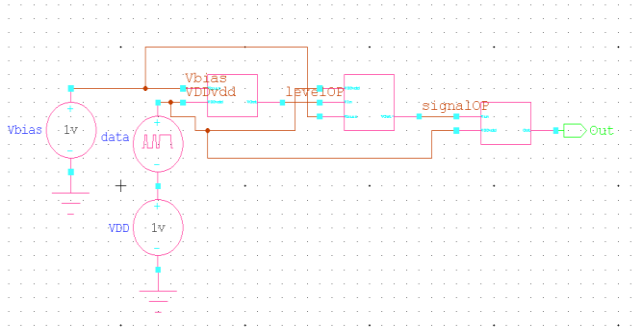

Fig. 14 Schematic diagram of the Proposed PLC Receiver

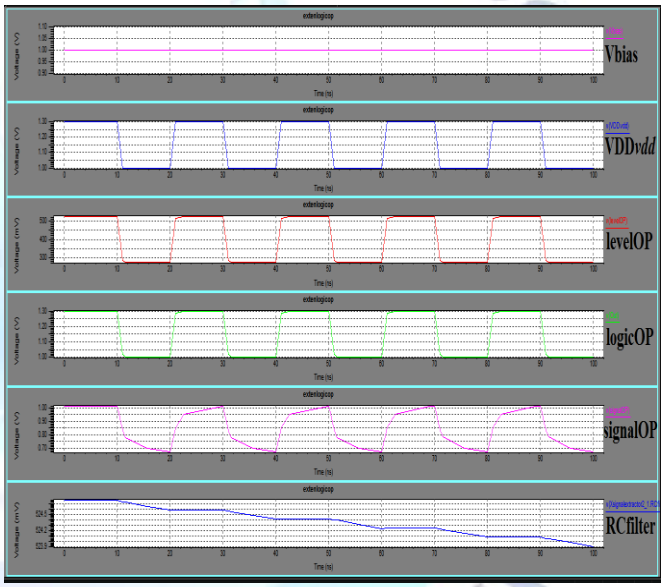

Fig. 15 PLC Receiver Transient Response

The top waveform is Vbais fixed voltage 1V. The second voltage waveform is a sequence of an input data signal 1010 superimposed on the supply voltage of 1.3V. The third waveform is the output of the level shifter. The fourth waveform is the output of the PLC receiver, which correctly reproduces the data sequence of 1010. The fifth waveform is the output of the signal extractor. And the bottom wave form is the response of the RC low pass filter.

Average power consumed for PLC receiver is 0.7690421771e-03 (m Watts).

The layout of the Proposed CMOS PLC Receiver is shown in Fig. 16

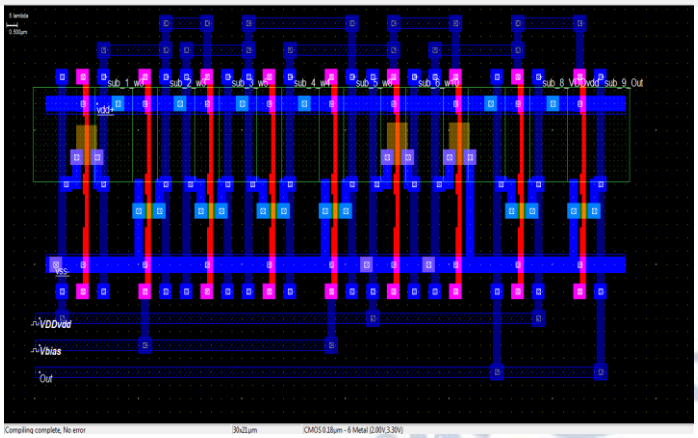

Fig.16 Proposed CMOS PLC Receiver Layout

V. CONCLUSION

The receiver mainly consists of three building blocks out of which the level shifter, the first block is responsible for shifting the data signal DC level to somewhat half of the supply level. The PSRR of the same is lowered to a smaller extend to make the output signal sensitive to the supply voltage. The signal extractor which is a differential amplifier along with a low pass filter in which a biased NMOS transistor and a capacitor are the main components is used to eliminate the DC value from the signal to mitigate the supply voltage variations and droops. The third block which is responsible for the noise immunity of the entire receiver is the Low Voltage CMOS Schmitt trigger and in which to contribute to the power reduction, and using a dynamic body biasing method.

The proposed work is a low voltage Schmitt trigger which is used for the power reduction and also the low power CMOS technique called the dynamic body biasing method could also contributed to achieve the aim. This new work reduces the power consumption which is to be 0.769mW.

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