Design of RAM using Pulsed Latch Based Shift Register

P. Mounika[1] | P. Soundarya mala[2]

[1]PG Scholar, Department of ECE, Godavari Institute of Engineering and Technology, Rajahmundry, Andhra Pradesh, India.
[2]Associate Professor, Department of ECE, Godavari Institute of Engineering and Technology, Rajahmundry, Andhra Pradesh, India.

ABSTRACT

In this paper proposed for low power area efficient for shift register based SRAM design using pulsed latches. The area, delay and power consumption reduced by flip-flop design replace with pulsed latches. In this method reduce the timing problem. In this paper proposed for 256 bit shift register SRAM. Verilog HDL has been used to implement the various blocks and simulation done using Xilinx simulator. RTL implementation has been done using Xilinx ISE suite 14.3.

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KEYWORDS: *RAM, Shift register, Pulsed latch, Low Power Design*

I. INTRODUCTION

Flip flops are the basic storage elements used appreciably in all sorts of digital designs. because the characteristic size of CMOS era method scaled down in keeping with Moore's law, designers are able to combine many numbers of transistors onto the equal die. The extra transistors there might be extra switching and more strength dissipated inside the shape of warmth or radiation. warmness is one of the phenomenon packaging challenges on this epoch, it's miles one of the fundamental challenges flow strength design methodologies and practices. another motive force of low strength research is the reliability of the integrated circuit. extra switching implies higher common modern is expelled and consequently the opportunity of reliability problems happening rises. we are shifting from laptops to drugs and even smaller computing digital structures. With this profound fashion persevering with and without a match trending in battery lifestyles expectancy, the greater low strength issues will ought to bead dressed. The contemporary traits will finally mandate low strength design automation on a very huge scale to match the tendencies of power consumption of today's and future integrated chips[3]. electricity intake of Very large Scale incorporated design is given by generalized relation, P = CV2f [1]. for the reason that strength is proportional to the square of the voltage as per the relation, voltage scaling is the most distinguished manner to reduce energy dissipation. but, voltage scaling is results in threshold voltage scaling which bows to the exponential growth in leakage energy. even though numerous contributions were made to the art of single side induced flip-flops, a want obviously happens for a layout that in addition improves the overall performance of unmarried facet triggered flip flops[2].patterns.

The structure of a shift register is quite easy. An N-bit shift sign in consists of collection connected N data flip-flops. The rate of the flip flop is less crucial than the area and power consumption due to the fact there may be no circuit between flip-flips in the shift sign in. The smallest turn-flop is appropriate for the shift register to lessen the place and electricity consumption. lately, pulsed latches have

replaced flip-flops in lots of applications, due to the fact a pulsed latch is tons smaller than a flip flop [6]–[9].but the pulsed latch can not be utilized in a shift sign in due to the timing problem between pulsed latches.

II. Proposed Pulse Latches

A master-slave flip-flop the use of latches in Fig. 1 may be replaced by using a pulsed latch which includes a latch and a pulsed clock signal fig four. For the pulsed clock sign all the pulsed latches proportion the heart beat technology circuit. Due to this sharing of the pulse clock circuit the area and power consumption intake of the circuits reduces to almost half of the master slave flip flop.

- It has a downside that the pulsed clock generator can't be used directly on this circuit because of its timing troubles.
- To overcome this numerous steps may be applied consisting of to add delay circuits between latches use multiple non-overlap delayed pulsed clock signals

All though both the above noted techniques resolve the timing hassle the postpone circuits gift project within the place and power intake area ,so it's far excellent within the hobby of low strength and region designing to utilize the non over lapping more than one not on time pulse clock indicators

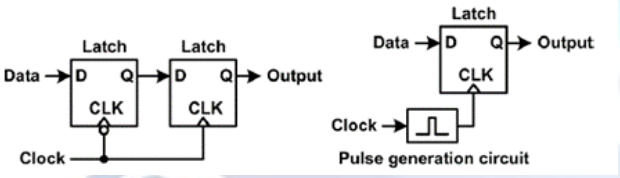

Fig1: Flip-flop and Pulsed latch

Pulse Generator:

Every pulsed clock sign arrives at the sub shift registers at different time because of the heartbeat skew within the wire. the heartbeat skew increases proportional to the wire distance from the delayed pulsed clock generator. All pulsed clock alerts have nearly the equal pulse skews while they arrive at the equal sub shift check in. consequently, inside the same sub shift sign in, the heart beat skew differences among the pulsed clock indicators are very small. The clock pulse durations larger than the pulse skew differences cancel out the outcomes of the heart beat skew differences. every other solution is to insert clock buffers and clock bushes to send the short clock pulse with a small wire postpone. How ever this increases the region and strength overhead. Further more, the more than one clock pulses make the more overhead for more than one clock buffers and clock timer.

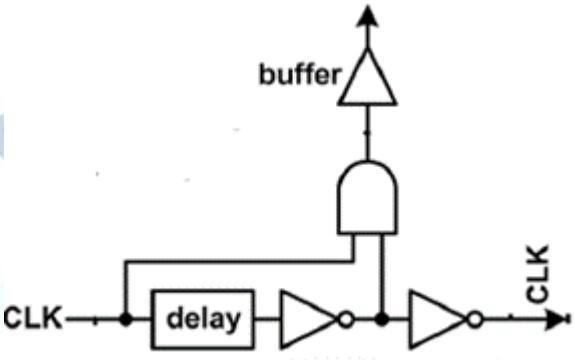

Fig2: Pulse generator

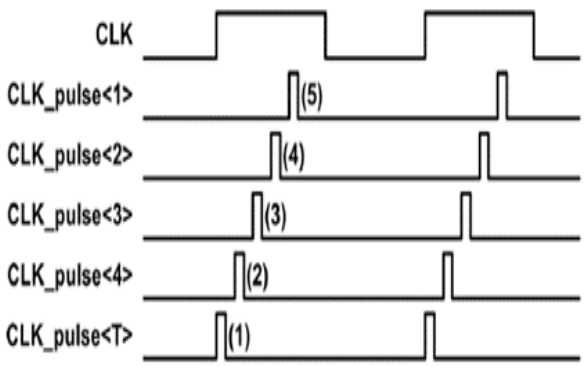

Fig:3 Pulsed clock signals

III. Proposed RAM Design

On this paper proposed for Shift check in using SRAM design with help of pulsed clock generators. The memory save the 256 bit facts's. static Random-get right of entry to reminiscence (RAM) can be a fashion of semiconductor memory that uses bi-solid latching electronic system to save every bit. The time period static differentiates it from dynamic RAM (DRAM) that must be sporadically invigorated. SRAM reveals understanding remembrance; but it is nevertheless unstable within the typical feel that information is eventually misplaced once the reminiscence is not steam-powered. For increasing the battery standby time I'm developing with a replacement fashion of RAM cell that consumes less power than the triumphing SRAMs. the key objective in the back of this paper is to cut back the facility consumption of random access memory.

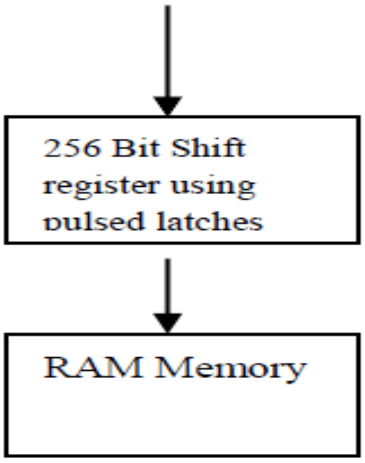

Fig4: RAM memory using shift register

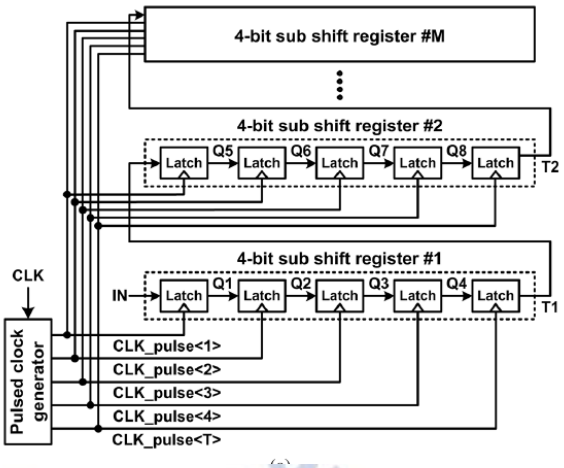

Fig5: Shift register

Write operation:

For writing 1/0 we should provide the data to the bit line (BL), with respect to the bit line bar (BL̄). When the word line (WL) is enabled the data is written into respective node.

Read Operation:

When the word line (WL) is enabled, the bit line which connected to the node of the cell containing '0' is discharged. Using sense amplifiers we can know the node containing 1/0 by sensing the bit lines. The bit line containing '1' means it's connected to the node containing '1' and vice versa.

Design Implementation:

While designing any circuit or chip it's vital to bear in mind different factors answerable for it to be implemented in actual existence. The most clock frequency in the conventional shift sign up is constrained to most effective the postpone of turn-flops due to the fact there is no delay between flip-flops. therefore, the vicinity and electricity consumption are more critical than the velocity for choosing the turn-flop. The proposed 256-bit shift register uses 4 latches and it plays shift operation with five non overlap not on time pulse clock signals (CLK_pulse). 256 latches store 256 bit statistics (Q1-Q256). The series of the pulsed clock signals is in the opposite sign of the four latches. The shift register outputs stored to SRAM circuits .finally the Shift register design get less area and less power consumption with help of pulsed clock generators.

IV. RESULTS

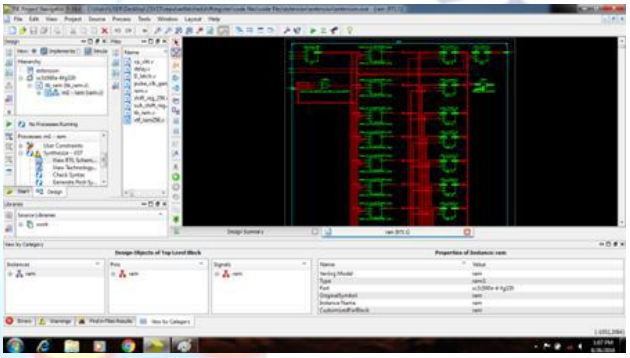

Fig:6 RTL schematic for shift register

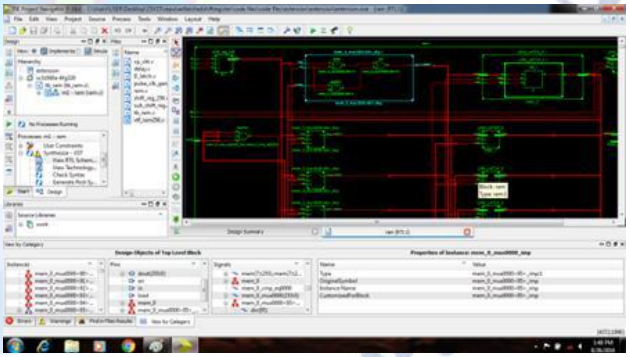

Fig: 7 RTL schematic for SRAM using shift register

Table 1: Power Analysis

Target devices	Kintex-xc7k70t
Leakage Power	0.080Watts

In this paper, we have proposed a novel deployment of all optical implementation of sequential circuits based on MZI functionality using reversible logic. The design of all optical implementation reversible counters is new one. Our design can be extended up to *n*-bit counter

also. By using this reversible logic functionality finite state machines can also be designed. Reversible logic has enormous advantages over conventional logic.

V. Conclusion

The timing problem between pulsed latches is solved using more than one non-overlap not on time pulsed clock indicators rather than a single pulsed clock sign. A small range of the pulsed clock indicators is utilized by grouping the latches to numerous sub shifter registers and the usage of extra transient garage latches. The implementation results of proposed and traditional architectures based totally on Xilinx FPGA Spartan XC3S200 are summarized.

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