A Novel Approach for High Speed Performance of Sequential Circuits using Reversible Logic Based on MZI

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ABSTRACT

The enhancement in the field of nanometer technology leads to minimize the power consumption of logic circuits. In order to that Reversible logic design has been one of the promising technologies gaining greater interest due to high speed performance and low power consumption. Due to its significant advantages reversible logic gates and combinational circuits has been proposed in optical domain using Semiconductor Optical Amplifier based Mach Zehnder interferometer switches. For all optical realization of reversible combinational circuits, an optical reversible MNOT and 4×4 Toffilo Gates are proposed for the first time in the literature. Multiplexer, De-multiplexer, Decoder and Adder circuits are designed using these proposed gates. In this paper, it presents a novel deployment of reversible logic sequential circuits using Semiconductor Optical Amplifier (SOA) based Mach-Zehnder Interferometer (MZI) switches, which includes the designs of D-Latch, Shift Registers, Synchronous and Asynchronous counters. The circuits are designed using minimum number of MZI switches. When compared to the conventional logic circuits the proposed design leads to reduction of the power consumption.

KEYWORDS: *Reversible computing, MZI, Shift Registers, Counter, Optical cost, Optical delay*

I. INTRODUCTION

The demand of high-performance computing has been increased by the growing technologies. As per the G.Moore's Law[23], it states that the number of transistor counts to be integrated per unit area in silicon will almost doubles in every two years. With the advanced improvements in semiconductor technology, there has been an increased emphasis in low power designing techniques over last few decades. Reversible computing process has been proposed by many researchers as a possible alternative to target the energy dissipation effect. Recently researchers have proposed different employments of various reversible logic circuits analysis in all-optical computing domain. Most of these works are based on SOA based MZI switches, which provides desirable features like ultra low power dissipation, fast switching. Reversible logic has become a popular emerging paradigm because of its applications in various technologies like DNA computing, optical computing, quantum computing etc. A reversible circuit consists of a cascade of basic reversible gates without any feedback or fan-out connections, and the equal number of inputs and outputs must be there. A photon can store information in a signal having zero rest mass in the optical domain, and provides very high speed performance. The properties of photon have motivated the researchers to study and develop the reversible circuits in optical domain. Theoretically from the old principles of Landauer and C.H.Bennett, reversible logic is considered as an alternative to low-power computation. Optical implementation of all

reversible gates can be possible as a one alternative to overcome the power dissipation problem in traditional computing. Also based on MZI implementation of reversible logic gates offers significant advantages like high speed, low power, ease of fabrication, and fast switching operation.

In this paper, all-optical implementation of sequential circuits using reversible logic are proposed. The sequential circuit is one of the most important components of the system and the memory element is a primary concern in this circuit. Lossless information is provided by using the reversible logic and no heat generation is occurred and an intensive research is still going on, on the design and implementation of the sequential circuit using reversible logic technology. To achieve high speed computation, high packaging density in the conventional logic circuits results in more heat dissipation. The conventional computing is found that it is not able to deal with low power consumption and heat dissipation issues of the current computing environment. In 1961, R. Laundaur has stated that heat dissipation and consumption occurs due to energy loss in traditional logics. Each bit dissipates an amount of energy equal to KTln2 joules (where K is Boltzmann's Constant and T is the absolute temperature). In 1973, C. H. Bannett stated that the heat dissipation can overcome by using the reversible technology of VLSI circuits. The reason for choosing reversible logic is the information of bits are not erased in reversible computing. Reversible Logic seems to be hopeful due to its wide applications in developing technologies such as quantum, optical computing and power efficient Nano-technologies etc. Loss of information cannot be occurred in reversible logic. A reversible logic gate has one to one mapping i.e. number of input lines are equal to number of output lines. In the reversible logic Fan-out is not permitted. Constant inputs and garbage output lines can be added to the circuit to make it reversible.

II. BACKGROUND

The reversible logic function [1-3] is a special and different type of logic function like traditional logic functions, it consists of bijective mapping between inputs to outputs. Reversible logic circuits are motivated in 1960s by theoretical considerations of zero-energy computation and also practical improvement of bit-manipulation transformation in cryptography technique and computer graphics. In 1980s, reversible circuits have attracted interest as components of quantum algorithms, and recently in photonic and nano-computing technologies where some of the switching devices offer no signal gain. In this section, the fundamentals of the reversible logic circuits are introduced. Next, the optical implementation of MZI switch and its working principle are described. Designing of basic reversible gates like CNOT Gate, Toffoli Gate, and Fredkin Gate by using MZI switches are presented [10-11].

A. Reversibility:

A fan-out free circuit (*Cnf*) with the circuit depth (*d*) over the set of input lines I ={*i1, i2, …,in*} is said to be reversible (*Rc*) if mapping from input to output is one-to-one and the number of inputs (*m*) should be equal to number of outputs (*n*) i.e. $m = n$ and also the circuit should consists only reversible gates (*gj*) i.e. *Cnf =g0.g1.g2. … .g(d-1),*where *gj* represents *j*th reversible gate of the circuit.

B. MZI Architecture:

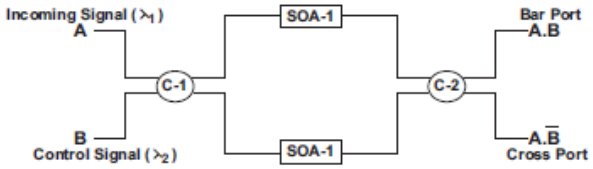
Designing of reversible logic gates like NOT, *k*-CNOT, Fredkin, Toffoli, Peres may possible in many ways. Among them, the quantum computing and optical technology are two different prominent. From the quantum computing technology point of view, the quantum gates such as NOT, C-NOT, V and V+ are used to implement the reversible logic gates. In optical domain, MZI based switches are used to design the optical reversible logic gates.

The optical MZI switch can be implemented using the following components: 2 Semiconductor Optical Amplifiers (SOA-1, SOA-2) and 2 couplers (C-1, C-2). MZI has two inputs ports, A & B and two output ports namely Bar port and Cross port, respectively as shown in Figure.1 The optical signals coming from the input side are port B and port A called as control signal (λ_2), and the incoming signal (λ_1), respectively. The working principle of a MZI switch is described below.

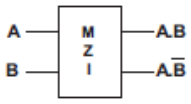
- When A=1 and B=1, i.e. incoming signal at port A and control signal at port B

are logic high, then the light appears at the output bar port but not at the output port (cross port).

- When A=1, B=0, i.e. the absence of control signal at input port B and presence of incoming signal at input port A then the light appear at the output cross port and but not at the output bar port is observed.
- In all other cases, i.e. when A=0, B=1 and A=0, B=0, no light appears at output ports namely bar port and cross port.



(a) Semiconductor Optical Amplifier based MZI



(b) Functional behavior of MZI switch

Fig. 1: SOA based MZI switch

The logic values of the absence and presence of the light are denoted by 0 and 1, respectively. From the perspective of Boolean operations, the above behavior of MZI switch is written as,

R (Bar Port) =*A.B* and

S (Cross Port) =*A*.B(bar)

C. Beam Combiner (BC) and Beam Splitter (BS):

Beam combiner (BC) combines the optical beam while the beam splitter (BS) will splits the optical beam into two separate optical beams. According to [11-12], the optical cost and the optical delay of beam splitters and beam combiners are very negligible.

D. Optical cost and delay

As the optical cost of Beam Splitter and Beam Combiner is comparatively small, the optical cost of a circuit is the number of MZI switches used to design for the realization. The Optical delay is estimated as the number of stages of the MZI switches multiplied by a unit Δ. Hence, calculating the optical cost of a circuit is assumed to be zero.

III. PREVIOUS METHOD

In the previous method, a new MNOT Gate is proposed and an all optical realization of 4×4 Toffilo Gate is also presented to design optimized optical reversible circuits. By using these proposed gates, some of the combinational circuits like all-optical Reversible 2×1 Multiplexer, 4×1 Optical Reversible Multiplexer, Reversible 4×1 De-Multiplexer, 3-to-8 Decoder circuit, Optical Reversible Gate(ORG-I) and The improved All-optical Reversible Full Adder Circuit are designed.

IV. PROPOSED METHOD

In this section, we present all optical implementation of D-latch, Shift Registers and Counters with the property of reversible functionality. To design the above sequential circuits, Semiconductor Optical Amplifier (SOA) based Mach-Zehnder Interferometer (MZI) switches used. Our main aim in this work is to achieve the reversible logic designing of counters with minimum number of MZI switches and ancilla lines.

I. MZI based D-Latch:

The implementation of all-optical MZI based D-Latch is proposed and presented using reversible logic and its schematic is shown in below figure.

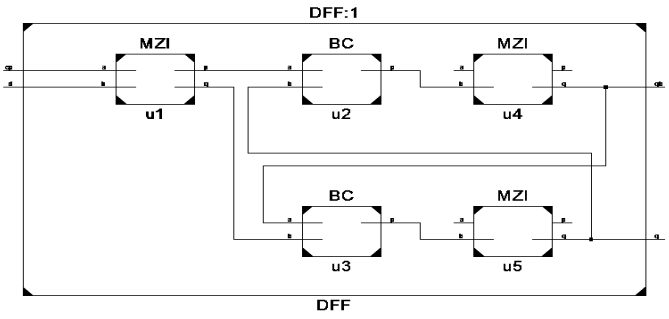


Fig.2: MZI based all optical implementation of D-Latch

II. MZI based Shift Registers:

This section describes the design and realization of all optical realization of shift register based on MZI switches. When we consider about the registers we have different types among those we are implementing shift registers such as serial-in-serial-out (shown in Fig.3a), serial-in-parallel-out (shown in Fig.3b),

parallel-in-serial-out (shown in Fig.3c) and parallel-in-parallel-out shift registers (shown in Fig.3b).

The shift register are another type of sequential logic circuits that can be used to transfer the data in the form of binary data. The name itself says that the data is transferred by shifting the inputs to the output at every clock cycle hence it is called shift register. Generally a shift register contains several number of single bit D-latches which carries either logic 1 or logic 0. And these latches are connected in a serial arrangement so, that the output from one latch becomes the input for another latch and so on. The data transfer movement of shift registers is done from left to right.

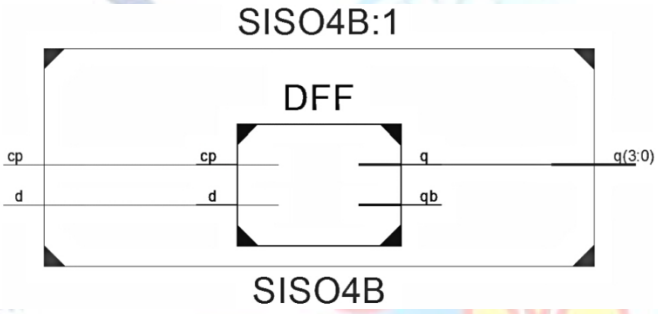


Fig.3a: MZI based Serial-in-serial-out schematic.

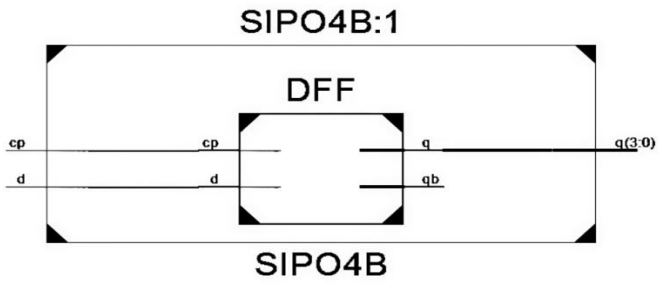


Fig.3b: MZI based Serial-in-parallel-out schematic

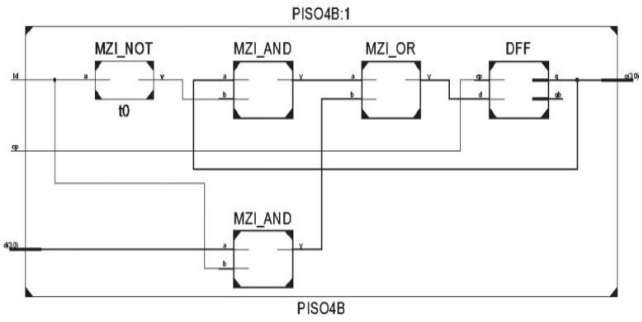


Fig.3c: MZI based Parallel-in-serial-out schematic

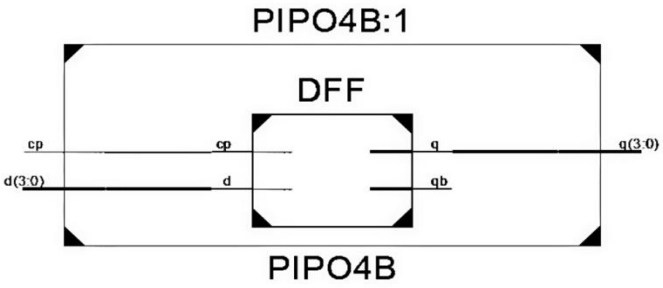


Fig.3d: MZI based Parallel-in-parallel-out schematic

III. Sequential Counters:

Also all optical implementation of MZI-based counters are implemented. In counters we have two different types known as asynchronous and synchronous counters.

A. Asynchronous Counters

Asynchronous counter is called as ripple counter. Design architecture and working principle of all optical, functionally reversible asynchronous down counter is explained here. The mathematical model for simulation of this counter is described below.

A.1. Design of 2-bit positive edge triggered down counter

In figure 4(a) it represents 2-bit positive edge triggered down counter base on MZI is depicted. It consists of two D flip-flops which are named as FF-0 and FF-1.

In each Flip-flop it contains three MZI switches MZ1-1, MZI-2, MZI-3 respectively and two beam couplers as BC-1 and BC-2. For splitting the beams we use beam splitters as BS-1, BS-2, BS-3 and BS-4.

The signal flow characteristics of the counter are shown in below figure 4(a). When we consider the first flip-flop FF-0, it consists of inputs signals as CP, D_0, and constant input 1. For the first MZI switch (MZI-1) the incoming signal is CP and control signal is D_0 and it produces two outputs as B1 at bar port, C1 at cross port. These 2 outputs are used as incoming signals for two beam couplers BC-1 and BC-2. Beam couplers combines the two signals, for BC-1 the inputs are one from at bar port of MZI-1, B1 and another input is from third MZI switch's (MZI-3) cross port output C3. For another beam coupler BC-2 has two inputs, one from MZI-1's cross port output C1 and other is from second MZI's cross port

output C2. By using the beam splitters we split a signal into to optical beams here the same splitter is used to split the constant input 1 for providing as an input for both MZI-1 and MZI-2 switches at incoming signal ports. The MZI-2 switch produces two outputs one is at bar port B2 and cross port C2 which is denoted as $Q_{0\ bar}$ as an output signal of FF-0 and this output. This Q_0 is feedback to D_0 input port and act as an incoming signal. The output from MZI-3 switch at cross port C3 is the Q_0 output signal. Similarly, the same design architecture of FF-0 is used for FF-1 designing. The input signals of FF-1 MZI-1 are from FF-0's Q_0 signal as incoming signal CP and D_1 as control signal. Once we obtained the both incoming and control signals for FF-1 the same design architecture is followed for this flip-flop.

A.2. Operational principle of 2-bit positive edge triggered down counter

The operational principle of asynchronous positive triggering down counter as shown in Fig 3(a) and its operation is described below.

Here, the switch presents output as follows, the presence of light is represented as logic high(1) state and absence of light is represented as logic low(0) state.

State I: Let the values of Q_0 and Q_1 be 0 i.e. Q_0=0 and Q_1=0. The value of $Q_{0\ bar}$ is directly connected to D_0, hence the D_0 value 1 and the value of clock pulse CP is also 1. Now both incoming signal and control signal of MZI-1 are present and according to MZI working principle light emits only at bar port and incidents on BC-1. From BC-1 output light will be emitted. There is no light emits at cross port of MZI-1 which is an input of BC-2. Now there is a constant input signal 1 as an incoming signal for MZI-2 and also we have output signal of BC-1 which acts as control signal of MZI-2. By following the same working principle of MZI we have no light emits at the cross port of MZI-2. Due to absence of light at C2 there is no input for BC-2 and the output of BC-2 emits no light at its output port. Also the control signal of MZI-3 is not present but due to presence of MZI-3 input signal at cross port, FF-0 receives a light signal at the output port which is the final result of Q_0, i.e. Q_0=1. Until here the operation of half of the counter is performed, from the final output Q_0 acts as MZI-1 incoming signal of FF-1 flip-flop. The input signals incoming and control signals of MZI-1 are present and its value of Q_0 and D_1 are logic high (1). Hence, the operation of FF-1 is same as the operation of FF-0, the output at cross port of MZI-3 produces light signal i.e. the final result is Q_1=1. Now, the next state becomes Q_1=1 and Q_0=1.

State II: Now, from the previous stage we have values of Q1=1 and Q0= 1. Again with clock pulse value CP=1 act as incoming signal and D0 (which is equals to the value of $Q_{0\ bar}$) as control signal of MZI-1 of FF-0. The only incoming signal is present at MZI-1, according to the working principle, at the cross port of MZI-1 of FF-0 emits light which incidents as an input of BC-2 and at the bar port of MZI-1 of FF-0 produces no light. So the signal of BC-2 is present that acts as control signal of MZI-3. The constant input 1 act as an incoming signal for MZI-3 so both the inputs signals are present for MZI-3 switch and it produces output at its cross port i.e. no light emits. The value of final output at the MZI-3, C3 is Q_0=0. This Q_0 acts as an incoming signal of MZI-1 of FF-1 flip-flop and input signal D_1 is connected to $Q_{1\ bar}$. At this condition the value of D_1 is logic low (0). As both of the incoming signal and control signal of MZI-1 of FF-1 are absent. Hence, no operation is done in FF-1 the final output of FF-1 does not change and it produces the same as the previous state's output value. The final output of FF-1 flip-flop is Q_1=1. Now, the next state becomes Q_1=1 and Q_0=0.

State III: Now, let us considering the values from the previous state the values are Q_1=1 and Q_0=0. The input signal D_0 is directly connected to $Q_{0\ bar}$ its value is logic high (1) and the clock pulse is also logic high(1) i.e. the incoming signal and control signal both are present at MZI-1 of FF-0 flip-flop. So the same condition of FF-0 first stage occurs in this situation. According to working principle of MZI, in very first stage, the final output of FF-0 flip-flop is logic high (1) i.e. Q_0=1. Now, this outputs signal of MZI-3 of FF-0, Q_0 acts as an incoming signal and the input signal D_1 is directly connected and the value of D_1=0. Here, incoming signal is only present at MZI-1 of FF-1 flip flop. The same situation of FF-0 second stage occurs at this condition. Hence, according to the MZI working principle of FF-0 as followed in the second stage, the final output signal value of FF-1 is logic low (0) i.e.

Q_1=0. Now, the next state becomes Q_1 has logic low and Q_0 has logic high values i.e. Q_1=0 and Q_0=1.

State IV: From the outputs of previous state this state has values of Q_1=0, Q_0=1 and the input signal D_0 which acts as control signal of MZI-1 of FF-0 is logic low (0). The value of clock pulse CP is logic high (1). There is an absence of control signal and incoming signal only is present at MZI-1 of FF-0. This condition is same as the second state of FF-0 flip-flop. Hence, according to working principle of MZI, the final output value of FF-0 is 0 i.e. Q_0=0. This Q_0 value acts as the incoming signal of MZI-1 of FF-1 and D_1 is directed towards to the complement of Q_1 i.e. $Q_{1\ bar}$ =1 and D_1=1. The incoming signal of MZI-1 in FF-1 is absence; hence there is no operation is done in FF-1 flop. The output value of FF-1 does not changed and it is same as Q1 previous state. Finally, the output of FF-1 is Q_1=0. Now, the next state becomes Q_1 has logic low and Q_0 has logic low values i.e. Q1=0 and Q0=0.

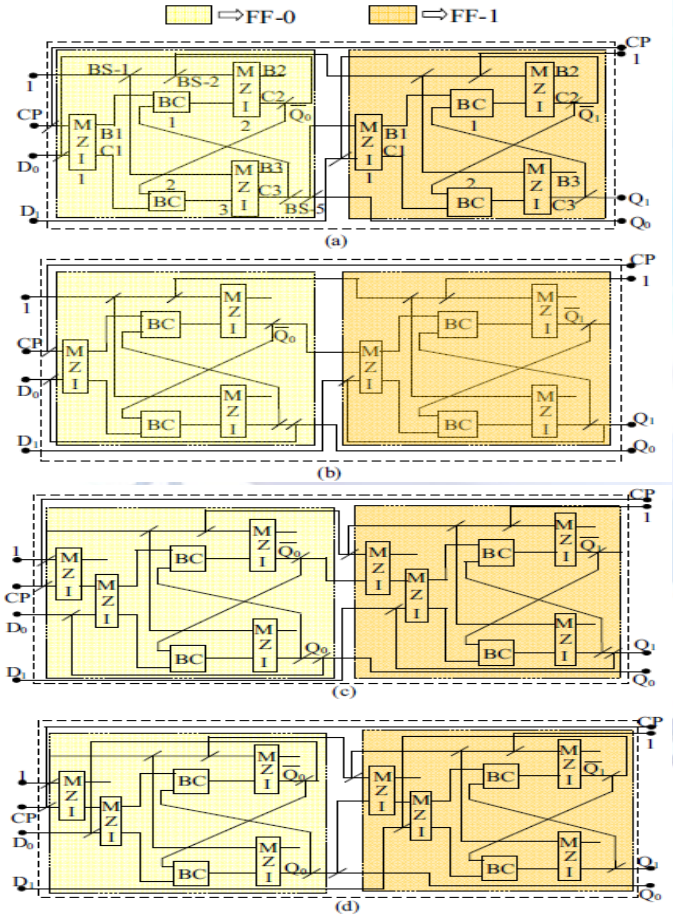


Fig. 4: Design of all optical reversible (a) asynchronous positive edge triggered down counter, (b) asynchronous positive edge-triggered up counter (c) asynchronous negative edge-triggered down counter (d) asynchronous negative edge-triggered up counter using MZI switch. BC: Beam Combiner; BS: Beam Splitter; CP: Clock Pulse

The states of the asynchronous positive edge-triggered counter are shown in Table-1.

Clock Pulse	FF-0				FF-1			
	CP_0	Q_0	D_0 $(\bar{Q}_0)$	Q_0^+	CP_1 (Q_0^+)	Q_1	D_1 $(\bar{Q}_1)$	Q_1^+
First	1	0	1	1	1	0	1	1
Second	1	1	0	0	0	0	1	1
Third	1	0	1	1	1	1	0	0
Fourth	1	1	0	0	0	0	1	0
Fifth	1	0	1	1	1	0	1	1

Table-1: Different States of Asynchronous Positive Edge-triggered Down Counter

The pictorial representation of positive edge triggered asynchronous up counter, negative edge triggered asynchronous down and up counter is depicted in Fig. 4(b), Fig 4(c), Fig 4(d), respectively. The flow chart of this simulation is shown in the below Fig.5.

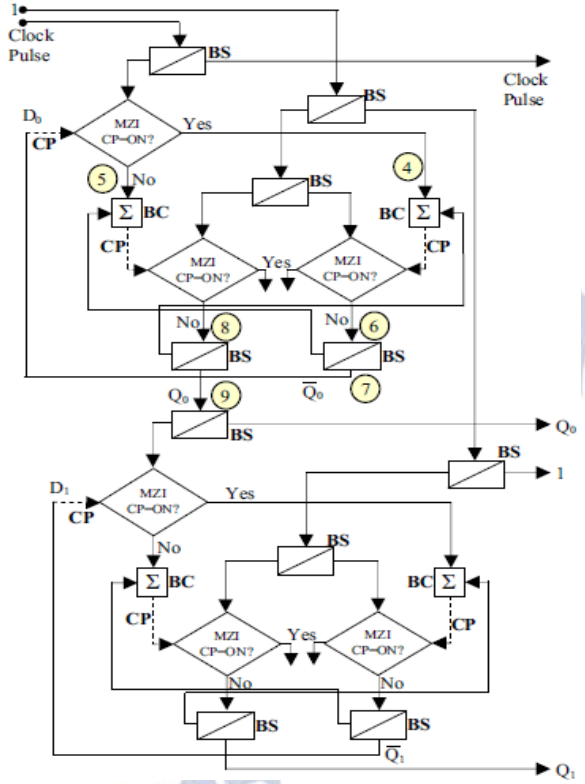


Fig.5: Control flow analysis of Asynchronous Positive edge-triggered down counter. CP: Control Pulse; BS: Beam Splitter; BC: Beam Combiner

B. Synchronous Counter

In the synchronous counters, all the flip-flops are triggered at a time. As we have already described the working principle of asynchronous positive edge triggered counter in detailed explanation, in this we represent only the pictorial representation of all optical

implementation of reversible architecture of MZI based synchronous up counter (negative edge triggered) and down counter (positive edge triggered) is shown in Fig. 6(a) and Fig. 6(b), respectively.

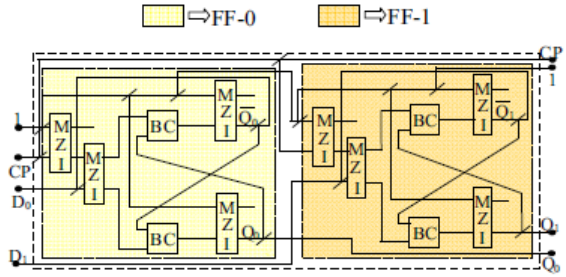


Fig. 6(a): Synchronous negative edge-triggered up counter implemented by MZI switch

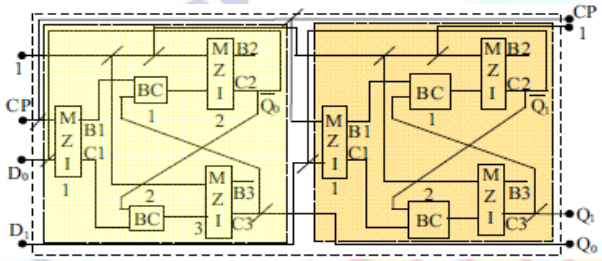


Fig. 6(b): Synchronous Positive edge-triggered down counter implemented by MZI switch.

It can be observed that the proposed designs have been optimized in terms of MZI switch BS and BC. Analysis of design complexities of all optical reversible counters is presented in Table-2.

Table-2: Analysis of design complexities of all optical reversible counters is presented

Table III: Analysis on design complexities of all optical reversible counters

Different types of *n*-bit counters		No. of MZI (Optical Cost)	No. of Beam Combiner	No. of Beam splitter	Garbage Output
Asynchronous	down counter (positive edge-triggered)	3*n*	2*n*	6*n*	4
	up counter(negative edge-triggered)	4*n*	2*n*	7*n*	6
Synchronous	up counter(negative edge-triggered)	4*n*	2*n*	7*n*	6
	down counter (positive edge-triggered)	3*n*	2*n*	6*n*	4

V. RESULTS

Using Verilog HDL the synthesis and simulation is done and these are performed on Xilinx ISE 14.4 version software tool. By making use of the waveforms, it is very easier to evaluate the effectiveness of the proposed architecture through simulation. Modelsim is used for simulation and Xilinx is used for evaluating the response for the existing and proposed architecture. By making use of this software tool we can see the outputs of these counters and also it views the design summary and synthesis report of every design architecture

VI. CONCLUSION AND FUTURE WORK

In this paper, we have proposed a novel deployment of all optical implementation of sequential circuits based on MZI functionality using reversible logic. The design of all optical implementation reversible counters is new one. Our design can be extended up to *n*-bit counter also. By using this reversible logic functionality finite state machines can also be designed. Reversible logic has enormous advantages over conventional logic.

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