Design of FIR Filter using Efficient Carry Select Adder

S. L. Sukanya[1] | N.M.L.R. Rao[2]

[1]PG Scholar, Department of ECE, Godavari Institute of Engineering and Technology, Rajahmundry, Andhra Pradesh, India.
[2]Associate Professor, Department of ECE, Godavari Institute of Engineering and Technology, Rajahmundry, Andhra Pradesh, India.

ABSTRACT

In this paper an efficient 8- Tapped FIR filter is designed using efficient Carry Select Adder and Wallace Tree Multiplier. Since in digital circuits complexity is increasing day by day efficient performance is the considerable parameter during designing of FIR filters and it is the main contributing factor for the popularity of the DSP systems. Two main operations of FIR filter are addition and multiplication so this paper concerns replacing the multiplier by Wallace tree multiplier and adder by efficient carry select adder in which all the redundant logic operations present in the conventional CSLA are eliminated and proposed a new logic formulation for CSLA. In the proposed adder, the carry select (CS) operation is scheduled before the calculation of final-sum, which is different from the conventional approach. In general Wallace tree multiplier is mostly preferred in order to reduce number of partial products. By employing the above 16- bit Carry Select Adder and 8 -bit Wallace Tree Multiplier an efficient 8- Tapped FIR filter is designed.

KEYWORDS: *FIR Filter, Carry Select Adder, Wallace tree multiplier, Low power Design*

I. INTRODUCTION

In recent times, many finite impulse reaction (FIR) clear out designs geared toward both low vicinity-price or excessive velocity or reduced strength intake are advanced [1]. we will observe that, with the increase in location, hardware cost of these FIR filters are growing. This commentary leads me to layout a low place-value FIR filter with the benefits of decreased energy consumption and slight velocity overall performance. To reduce the hardware value, the hardware place must be optimized. Multipliers eat the most quantity of area in a FIR clear out layout. manufactured from two numbers has twice the original bit width of the extended numbers. we can truncate the product bits to the required precision to reduce the vicinity cost [1]-[2]. conventional multipliers are changed through a modified booth multiplier right here. changed Wallace tree and dadda set of rules. It produces best half of the number of partial merchandise (PPs) while compared with an normal binary multiplication. modified sales space encoding (MBE) scheme is diagnosed because the most green booth encoding and deciphering scheme. The truncation mistakes for a modified sales space multiplication isn't always more than 1 ulp (unit of remaining area or unit of least precision). So there's no want of blunders reimbursement circuits.

II. DESIGN OF FIR FILTER

The FIR filter expressed as

$$y(n) = \sum_{k=0}^{N} X(n-k) * H(k)$$

y(n)=Output signals of FIR filter
X(n)-→ Input signals
H(k)-→set of coefficients
The implementation of FIR filters need multiplication, adder and signal delay. The

multiplication implemented by using Wallace tree and dadda algorithms. The adder circuit designed by area and delay based carry select adder circuits. basic structure mention in below figure.

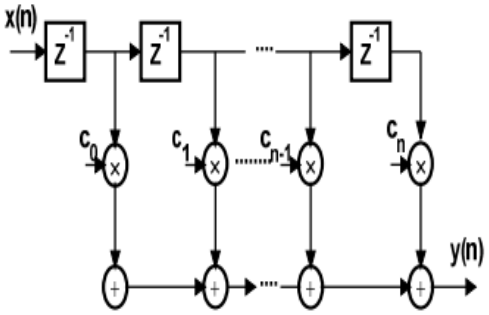


Fig:1 FIR Filter Design

III. PROPOSED FIR FILTER

In this paper proposed FIR filter is designed using Carry Select adder and Wallace tree multiplier .

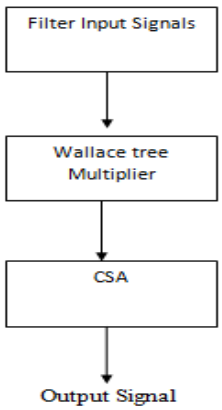


Fig:2 Flow of FIR Design

New Carry Select Adder Design:

The new CSLA is primarily based at the circuit layout shape is shown in Fig. three. It includes one HSG unit, one FSG unit, one CG unit, and one CS unit. The CG unit is composed of two CGs (CG0 and CG1) similar to input-convey '0' and '1'. The HSG gets n-bit operands (A and B) and generate half-sum phrase s0 and half-carry word c0 of width n bits each. both CG0 and CG1 receive s0 and c0 from the HSG unit and generate n-bit complete-convey words c01 and c11 corresponding to enter-deliver 0' and '1', respectively. The good judgment diagram of the HSG unit is proven in Fig.The common sense circuits of CG0 and CG1 are optimized to take advantage of the constant input-carry bits.

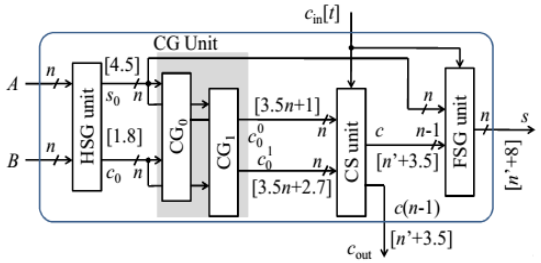


Fig:3 New Carry select adder design

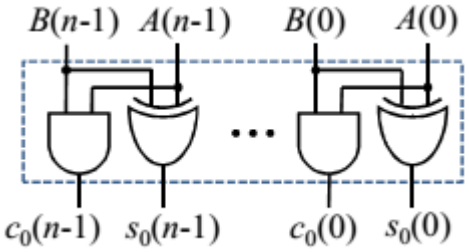


Fig:4 Half Sum Generator (HSG)

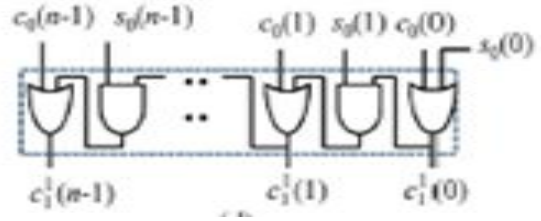


Fig:5 cg0 unit

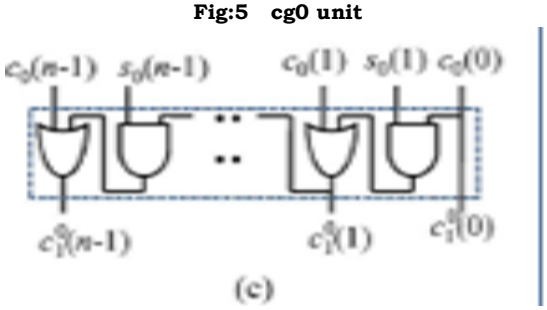


Fig:6 cg1 unit

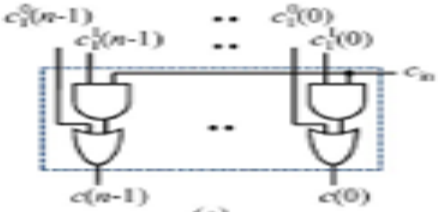


Fig:7 cs unit

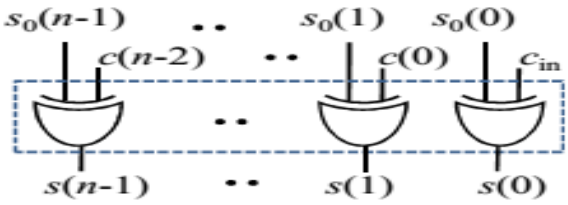


Fig:8 Full Sum Generator (FSG)

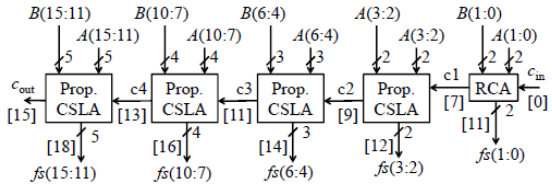


Fig:9 16 Bit Carry select adder Design

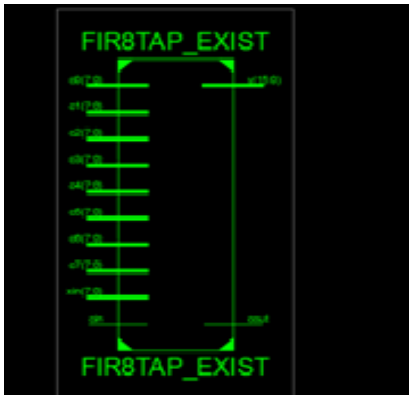
Wallace Tree Multiplier:

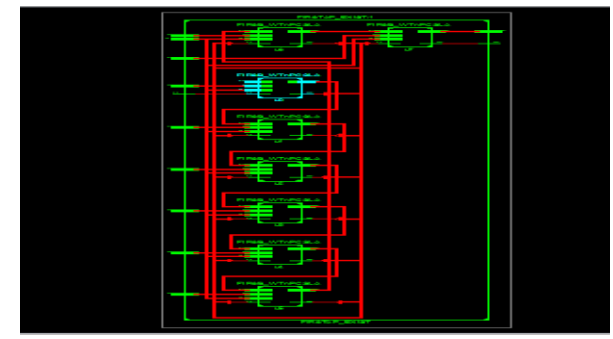
To reduces the quantity of partial merchandise to be introduced into 2 final intermediate outcomes we use Wallace tree. The primary operation of Wallace tree is multiplication of unsigned integer, an efficient hardware to implement a digital circuit that multiplies two integers is Wallace tree multiplier, designed with the aid of an Australian computer Scientist Chris in 1964.

Fig:10 Wallacetreemultiplier

Wallace tree is a good hardware implementation of a digital circuit that multiplies integers. Wallace tree is abnormal shape in that the informal description does no longer specify a systematic technique for the compressor interconnections. However nonetheless it's far an green implementation of adding partial products in parallel. Using this technique, a 3 step procedure is used to multiply two integer numbers. First step is to multiply each bit of one of the arguments, via every little bit of the alternative, yielding n 2 effects. Based totally on the placement of the multiplied bits, the wires carry extraordinary weights. The second step is to reduce the range of partial merchandise to two by using layers of full and half adders. The third steps are to institution the wires in two numbers, and then add them with traditional adder. There are two exceptional architectures of Wallace tree multiplier are to be had. First one is designed the usage of best half adder and complete adder, even as the second makes use of a more state-of-the-art carry skip adder (CSA). Wallace Tree Multiplier the use of simplest complete and half Adders is hired. With this concept of Wallace tree method is to reduce the quantity of adders by way of minimizing the quantity of the half of adder in any multiplier. the primary partial product is the least tremendous bit in the output of the multiplier result. After that, transferring to the next column of the partial product if there are any adders from the preceding product, the total Adder is used in any other case a halfadder is used and so on[13]. Wallace Tree Multiplier using carry bypass Adder is likewise hired. A deliver-skip adder consists of a easy ripple convey-adder with a unique speed up carry chain referred to as a skip chain. The purpose of the usage of the CSA is to enhance the worst case route delay. A four -bit CSA is used for imposing the Wallace tree multiplier. The carry output from the primary addition is the deliver enter inside the 2nd addition. The benefit of the use of CSA is to increase the most frequency. The Wallace tree multiplier the usage of CSA occupies smallest area even as the Vedic multiplier the usage of KSA consumes massive area. The strength intake of the four multipliers is convergent. inside the parallel FIR clear out. architecture, Wallace tree multiplier the use of CSA has the minimal critical direction while the Vedic multiplier the usage of conventional adder has the most delay.

IV. RESULTS





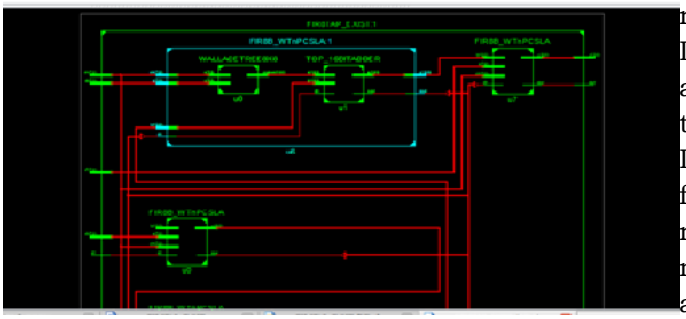


Fig:11 RTL Schematic for FIR Filter

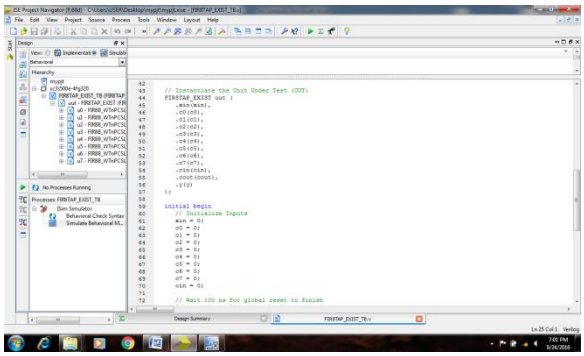


Fig:12 Test Bench waveform

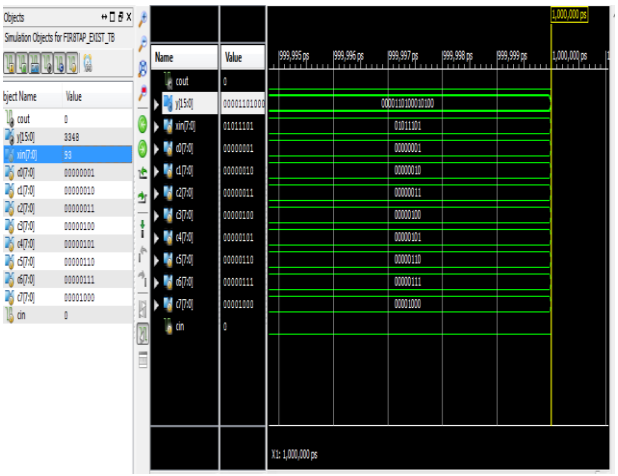


Fig:13 Waveform for FIR Filter

V. TABULATION

Target devices	Leakage power
Spartan-3E	0.0081Watts

VI. CONCLUSION

In this paper, an efficient fir filter is implemented using an efficient carry select adder and Wallace tree multiplier . Wallace tree multiplier delivers better performance than Dadda multiplier for the FIR filter architectures. The Wallace tree multiplier has the smallest critical path delay as compared to Dadda multiplier. Here the input samples and filter coefficients are applied as inputs to the multiplier and adders. The implementation results of proposed and traditional architectures based totally on Xilinx FPGA Spartan XC3S200 are summarized.

REFERENCES

[1] Design of a Power Optimal Reversible FIR Filter for Speech Signal Processing," IEEE Transactions On Signal Processing, Vol. 51, No. 2, Feb. 2003.

[2] Richard Hartley, "Optimization Of Canonic Signed Digit Multipliers For Filter Design," IEEE International Sympoisum on Circuits and Systems, Vol. 4, Jun 1991.

[3] C.R.Baugh and B.A. Wooley, "A two's complement parallel array multiplication algorithm," IEEE Trans. On Computers, vol.22, pp. 1045-1047, 1973.

[4] K.A.C.Bickerstaff, E.E.Swartzlander Jr., and M.J.Schulte, "Analysis of column compression multipliers," 15th IEEE Symp. On Computer Architecture, pp.33-39, 2001.

[5] C.S.Wallace, "A suggestion for a fast multiplier," IEEE Trans. On Computers, vol. 13, pp. 14-17, 1964.

[6] E.E. Swartzlander Jr., "Merged arithmetic," vol.29, pp. 946-950, 1980.

[7] S. White, "Applications of Distributed Arithmetic to Digital Signal Processing: A Tutorial Review," IEEE ASSP Magazine, July 1989, pp. 4 –

[8] Keshab K.Parhi, "VLSI Digital Signal Processing," Wiley.