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# Three phase Nine Level Inverter with Minimum Number of Power Electronic Components

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## ABSTRACT

*This paper presents a new configuration of a three-phase nine-level multilevel voltage-source inverter. This topology constitutes three-phase two-level bridge with three bidirectional switches. A multilevel dc link using fixed dc voltage supply and cascaded half-bridge is connected in such a way that the proposed inverter outputs the required output voltage levels. This topology has the advantage of increasing the number of voltage levels with reduced number of power electronic components. For the purpose of increasing the number of voltage levels with fewer number of power electronic components, the extended structure suggests different methods to determine the magnitudes of utilized dc voltage supplies. The proposed multi-level inverter is designed and implemented in MATLAB/SIMULINK, and required number of voltage levels are obtained.*

**KEYWORDS:** *Bidirectional switch, Cascaded Half-Bridge, multilevel inverter.*



## I. INTRODUCTION

Multilevel inverter has become more famous over previous years in high power electric applications without the usage of a transformer and filters [1].Multi-level inverters consist of a group of switching devices and dc voltage supplies, the output of which produces voltages with stepped waveforms. Multilevel technology has started with the three-level converter followed by numerous multilevel converter topologies. Multilevel inverters can be categorized into three topologies [2]-[3], they are, diode-clamped, flying-capacitor and cascaded H-bridge cell. Apart from these three main topologies, topologies are introduced [6]–[9]. Recently, asymmetrical and hybrid multistage topologies are becoming one of the most interested research area. In the asymmetrical configurations, the magnitudes of dc voltage supplies are unequal. These topologies reduce the cost and size of the inverter and improve the reliability since minimum number of power electronic components, capacitors, and dc supplies are used. The hybrid multistage converters consist of different multilevel configurations with unequal dc voltage supplies. Comparing to the unidirectional one, bidirectional switch is able to conduct the current and withstanding the voltage in both directions. Bidirectional switches with an appropriate control technique can improve the performance[10]-[11] of multilevel inverters in terms of reducing the number of semiconductor components, minimizing the withstanding voltage and achieving the desired output voltage with higher levels [12]–[15]this paper suggests a novel topology for a three-phase nine-level multilevel inverter. The number of switching devices, insulated-gate driver circuits, and installation area and cost are significantly reduced. The magnitudes of the utilized dc voltage supplies have been selected in a way that brings the high number of voltage level with an effective application of a fundamental frequency staircase modulation technique. Extended structure for *N*-level is also presented and compared with the conventional well-known multilevel inverters.

Simulation and hardware results are given and explained.

## II. Proposed Method

Fig. 1 shows the typical configuration of the proposed three-phase nine-level multilevel inverter.

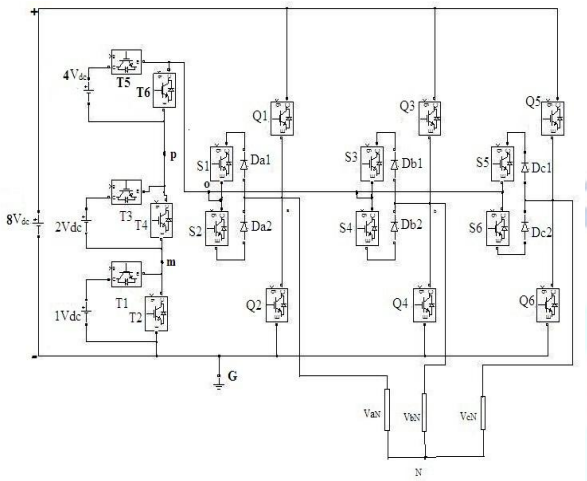


**Fig:1. Circuit diagram of the proposed three-phase nine-level multilevel inverter.**

Three bidirectional switches (S1–S6, Da1–Dc2), two switches–two diodes type, are added to the conventional three-phase two-level bridge (Q1–Q6). The function of these bi-directional switches is to block the higher voltage and ease current flow to and from the midpoint (o). A multi-level dc link built by a single dc voltage supply with fixed magnitude of 8 *V*dc and CHB having three unequal dc voltage supplies of *V*dc , 2 *V*dc and 4$V_{dc}$ are connected to (+, –, o) bridge terminals. Based on the desired number of output voltage levels, a number of CHB cells are used. Since the proposed inverter is designed to achieve nine voltage levels, the power circuit of the CHB makes use of three series cells having three unequal dc voltage supplies. In each cell, the two switches are turned ON and OFF under inverted conditions to output two different voltage levels. The first cell dc voltage supply *V*dc is added if switch T1 is turned ON leading to *V*mg =+*V*dc where *V*mg is the voltage at node (*m*) with respect to inverter ground (*g*) or bypassed if switch T2 is turned ON leading to *V*mg =0. Likewise, the second cell dc voltage supply 2 *V*dc is added when switch T3 is turned ON resulting in *V*om =+2$V_{dc}$. Where *V*om is the voltage at midpoint (*o*) with respect to node (*m*) or bypassed when switch T4 is turned ON resulting in *V*om = 0.similarly,the third cell dc voltage is added when switch T5 is turned ON resulting in Vop=+4$V_{dc}$. Where *V*op is the voltage at midpoint (*o*) with respect to node (*p*) or bypassed when switch T6 is turned ON resulting in *V*op = 0. The peak voltage rating of the switches of the conventional two level bridge (Q1–Q6) is 8 *V*dc whereas the bidirectional switches (S1–S6) have a peak voltage rating of 7 *V*dc. In CHB cells, the peak voltage rating of third cell switches is second cell switches (T3 and T4) is 2 *V*dc while the peak voltage rating of T1 and T2 in the first cell is *V*dc. By considering phase *a*, the operating status of the switches and the inverter line-to-ground voltage *V*ag are given in Table I.

It is easier to define the inverter line-to-ground voltages *V*ag, *V*bg , and *V*cg in terms of switching states *Sa*, *Sb*, and *Sc as*

$$\begin{bmatrix} Vag \\ Vbg \\ Vcg \end{bmatrix} = \frac{4Vdc}{N-1} * \begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix}$$

**Table 1**
**Switching State $S_a$ and Inverter Line to ground $V_{ag}$**

| Sa | Q1 | S1 | S2 | Q2 | T1 | T2 | T3 | T4 | T5 | T6 | Vag |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | OFF | OFF | OFF | ON | OFF | ON | OFF | ON | OFF | ON | 0 |
| 1 | OFF | ON | ON | OFF | ON | OFF | OFF | ON | OFF | ON | 1Vdc |
| 2 | OFF | ON | ON | OFF | OFF | ON | ON | OFF | OFF | ON | 2Vdc |
| 3 | OFF | ON | ON | OFF | ON | OFF | ON | OFF | OFF | ON | 3Vdc |
| 4 | OFF | ON | ON | OFF | OFF | ON | OFF | ON | ON | OFF | 4Vdc |
| 5 | OFF | ON | ON | OFF | ON | OFF | OFF | ON | ON | OFF | 5Vdc |
| 6 | OFF | ON | ON | OFF | OFF | ON | ON | OFF | ON | OFF | 6Vdc |
| 7 | OFF | ON | ON | OFF | ON | OFF | ON | OFF | ON | OFF | 7Vdc |
| 8 | ON | OFF | OFF | OFF | OFF | ON | OFF | ON | OFF | ON | 8Vdc |

where $N = 9$ is the maximum number of voltage levels.

The balanced load voltages can be achieved if the proposed inverter operates on the switching states depicted in Table II.

The inverter may have 48 different modes within a cycle of the output waveform. According to Table II, it can be noticed that the bidirectional switches operate in 43 modes. For each mode, there is no more than one bidirectional switch in on-state.

where $V$ab, $V$bc, and $V$ca are related to $V$ag, $V$bg , and $V$cg by

$$\begin{bmatrix} Vab \\ Vbc \\ Vca \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} Vag \\ Vbg \\ Vcg \end{bmatrix}$$

The inverter line-to-neutral voltages $V$aN, $V$bN, and $V$cN may be expressed as

$$\begin{bmatrix} VaN \\ VbN \\ VcN \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} Vag \\ Vbg \\ Vcg \end{bmatrix}$$

**Table-II**

**Switching State Sequence Of The Proposed Inverter Within One Cycle**

| $S_a$ $S_b$ $S_c$ | Period T(s) | ON Switches Leg a | ON Switches Leg b | ON Switches Leg c | ON Switches Cascaded Half-Bridge | $V_{ag}$ (v) | $V_{bg}$ (v) | $V_{cg}$ (v) |
|---|---|---|---|---|---|---|---|---|
| 8 0 0 | t1 | Q1 | Q4 | Q6 | T2,T4,T6 | $8V_{dc}$ | 0 | 0 |
| 8 1 0 | t2 | Q1 | S3,S4 | Q6 | T1,T4,T6 | $8V_{dc}$ | $V_{dc}$ | 0 |
| 8 2 0 | t3 | Q1 | S3,S4 | Q6 | T2,T3,T6 | $8V_{dc}$ | $2V_{dc}$ | 0 |
| 8 3 0 | t4 | Q1 | S3,S4 | Q6 | T1,T3,T6 | $8V_{dc}$ | $3V_{dc}$ | 0 |
| 8 4 0 | t5 | Q1 | S3,S4 | Q6 | T2,T4,T5 | $8V_{dc}$ | $4V_{dc}$ | 0 |
| 8 5 0 | t6 | Q1 | S3,S4 | Q6 | T1,T4,T5 | $8V_{dc}$ | $5V_{dc}$ | 0 |
| 8 6 0 | t7 | Q1 | S3,S4 | Q6 | T2,T3,T5 | $8V_{dc}$ | $6V_{dc}$ | 0 |
| 8 7 0 | t8 | Q1 | S3,S4 | Q6 | T1,T3,T5 | $8V_{dc}$ | $7V_{dc}$ | 0 |
| 8 8 0 | t9 | S1,S2 | Q3 | Q6 | T1,T4,T6 | $8V_{dc}$ | $8V_{dc}$ | 0 |
| 7 8 0 | t10 | S1,S2 | Q3 | Q6 | T1,T3,T5 | $7V_{dc}$ | $8V_{dc}$ | 0 |
| 6 8 0 | t11 | S1,S2 | Q3 | Q6 | T2,T3,T5 | $6V_{dc}$ | $8V_{dc}$ | 0 |
| 5 8 0 | t12 | S1,S2 | Q3 | Q6 | T1,T4,T5 | $5V_{dc}$ | $8V_{dc}$ | 0 |
| 4 8 0 | t13 | S1,S2 | Q3 | Q6 | T2,T4,T5 | $4V_{dc}$ | $8V_{dc}$ | 0 |
| 3 8 0 | t14 | S1,S2 | Q3 | Q6 | T1,T3,T6 | $3V_{dc}$ | $8V_{dc}$ | 0 |
| 2 8 0 | t15 | S1,S2 | Q3 | Q6 | T2,T3,T6 | $2V_{dc}$ | $8V_{dc}$ | 0 |
| 1 8 0 | t16 | S1,S2 | Q3 | Q6 | T1,T4,T6 | $1V_{dc}$ | $8V_{dc}$ | 0 |
| 0 8 0 | t17 | S1,S2 | Q3 | Q6 | T2,T4,T6 | 0 | $8V_{dc}$ | 0 |
| 0 8 1 | t18 | Q2 | Q3 | S5,S6 | T1,T4,T6 | 0 | $8V_{dc}$ | $1V_{dc}$ |
| 0 8 2 | t19 | Q2 | Q3 | S5,S6 | T2,T3,T6 | 0 | $8V_{dc}$ | $2V_{dc}$ |
| 0 8 3 | t20 | Q2 | Q3 | S5,S6 | T1,T3,T6 | 0 | $8V_{dc}$ | $3V_{dc}$ |
| 0 8 4 | t21 | Q2 | Q3 | S5,S6 | T2,T4,T5 | 0 | $8V_{dc}$ | $4V_{dc}$ |
| 0 8 5 | t22 | Q2 | Q3 | S5,S6 | T1,T4,T5 | 0 | $8V_{dc}$ | $5V_{dc}$ |
| 0 8 6 | t23 | Q2 | Q3 | S5,S6 | T2,T3,T5 | 0 | $8V_{dc}$ | $6V_{dc}$ |
| 0 8 7 | t24 | Q2 | Q3 | S5,S6 | T1,T3,T5 | 0 | $8V_{dc}$ | $7V_{dc}$ |
| 0 8 8 | t25 | Q2 | Q3 | S5,S6 | T1,T4,T6 | 0 | $8V_{dc}$ | $8V_{dc}$ |
| 0 7 8 | t26 | Q2 | S3,S4 | Q5 | T1,T3,T5 | 0 | $7V_{dc}$ | $8V_{dc}$ |
| 0 6 8 | t27 | Q2 | S3,S4 | Q5 | T2,T3,T5 | 0 | $6V_{dc}$ | $8V_{dc}$ |
| 0 5 8 | t28 | Q2 | S3,S4 | Q5 | T1,T4,T5 | 0 | $5V_{dc}$ | $8V_{dc}$ |
| 0 4 8 | t29 | Q2 | S3,S4 | Q5 | T2,T4,T5 | 0 | $4V_{dc}$ | $8V_{dc}$ |
| 0 3 8 | t30 | Q2 | S3,S4 | Q5 | T1,T3,T6 | 0 | $3V_{dc}$ | $8V_{dc}$ |
| 0 2 8 | t31 | Q2 | S3,S4 | Q5 | T2,T3,T6 | 0 | $2V_{dc}$ | $8V_{dc}$ |
| 0 1 8 | t32 | Q2 | S3,S4 | Q5 | T1,T4,T6 | 0 | $1V_{dc}$ | $8V_{dc}$ |
| 0 0 8 | t33 | Q2 | Q4 | Q5 | T2,T4,T6 | 0 | 0 | $8V_{dc}$ |
| 1 0 8 | t34 | S1,S2 | Q4 | Q5 | T1,T4,T6 | $1V_{dc}$ | 0 | $8V_{dc}$ |
| 2 0 8 | t35 | S1,S2 | Q4 | Q5 | T2,T3,T6 | $2V_{dc}$ | 0 | $8V_{dc}$ |
| 3 0 8 | t36 | S1,S2 | Q4 | Q5 | T1,T3,T6 | $3V_{dc}$ | 0 | $8V_{dc}$ |
| 4 0 8 | t37 | S1,S2 | Q4 | Q5 | T2,T4,T5 | $4V_{dc}$ | 0 | $8V_{dc}$ |
| 5 0 8 | t38 | S1,S2 | Q4 | Q5 | T1,T4,T5 | $5V_{dc}$ | 0 | $8V_{dc}$ |
| 6 0 8 | t39 | S1,S2 | Q4 | Q5 | T2,T3,T5 | $6V_{dc}$ | 0 | $8V_{dc}$ |
| 7 0 8 | t40 | S1,S2 | Q4 | Q5 | T1,T3,T5 | $7V_{dc}$ | 0 | $8V_{dc}$ |
| 8 0 8 | t41 | Q1 | Q4 | Q5 | T1,T4,T6 | $8V_{dc}$ | 0 | $8V_{dc}$ |
| 8 0 7 | t42 | Q1 | Q4 | S5,S6 | T1,T3,T5 | $8V_{dc}$ | 0 | $7V_{dc}$ |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 8 0 6 | t43 | Q1 | Q4 | S5,S6 | T2,T3,T5 | $8V_{dc}$ | 0 | $6V_{dc}$ |
| 8 0 5 | t44 | Q1 | Q4 | S5,S6 | T1,T4,T5 | $8V_{dc}$ | 0 | $5V_{dc}$ |
| 8 0 4 | t45 | Q1 | Q4 | S5,S6 | T2,T4,T5 | $8V_{dc}$ | 0 | $4V_{dc}$ |
| 8 0 3 | t46 | Q1 | Q4 | S5,S6 | T1,T3,T6 | $8V_{dc}$ | 0 | $3V_{dc}$ |
| 8 0 2 | t47 | Q1 | Q4 | S5,S6 | T2,T3,T6 | $8V_{dc}$ | 0 | $2V_{dc}$ |
| 8 0 1 | t48 | Q1 | Q4 | S5,S6 | T1,T4,T6 | $8V_{dc}$ | 0 | $1V_{dc}$ |

The simulated voltage waveforms of *V*ag, *V*ab, and *V*aN based on are shown in Fig.4,5 nd 6. where, for instance, 13 sequent voltage steps are seen in *V*aN waveform as follows: $16V_{dc}/3$, $15V_{dc}/3$, $14V_{dc}/3$, $13V_{dc}/3$, $12\ V_{dc}/3$, $11V_{dc}/3$, $10V_{dc}/3$, $9V_{dc}/3$, $8\ V_{dc}/3$, $6\ V_{dc}/3$, $4V_{dc}/3$, $2V_{dc}/3$, $0$,- $2V_{dc}/3$, -4 $V_{dc}/3$, -6 $V_{dc}/3$, -8 $V_{dc}/3$, $-9V_{dc}/3$, $-10V_{dc}/3$,$-11V_{dc}/3$, -12 $V_{dc}/3$, $-13V_{dc}/3$, $-14V_{dc}/3$, $-15V_{dc}/3$, $-16V_{dc}/3$. It is worth noting that all simulated waveforms are obtained at $t1=t2 = \ldots = t24 = 0.02/24$ s.

### III. Extended Structure

It is noticeable that there is possibility to reach an output voltage with higher number of steps in the proposed multi-level N inverter by extending the CHB circuit. Such extending can be done by adding more half-bridge cells connected in series as shown in Fig. In order to achieve the desired number of voltage levels, three methods can be followed to determine the magnitudes of utilized dc voltage supplies.

1) All cells have an equal dc supply in magnitude.

$$V_{dc1} = V_{dc2} = \ldots = V_{dcn} = V_{dc}$$

Then, the magnitude of fixed dc supply can be chosen as

$$V_{fix} = (N\text{-}1)\ V_{dc} = (1+n)\ V_{dc}$$

where $n$ is the number of utilized cells. The maximum number of voltage steps is related to the number of utilized cells by

$$N=n+2$$

The number of operation modes that makes the switching states sequence achieves the required output voltage waveform can be expressed as

$$M= 6(N\text{-}1)$$

2)The magnitude of dc voltage supply used in each and every cell in a particular inverter is obtained as follows:

$$V_{dc1}=V_{dc}$$
$$V_{dc2} =2V_{dc}$$
$$V_{dcn} = nV_{dc}$$
$$V_{fix} =(N\text{-}1)V_{dc}=1+\left[\frac{n(n+1)}{2}\right] V_{dc}$$
$$N=2+\left[\frac{n(n+1)}{2}\right]$$
$$M= 6(N\text{-}1)$$

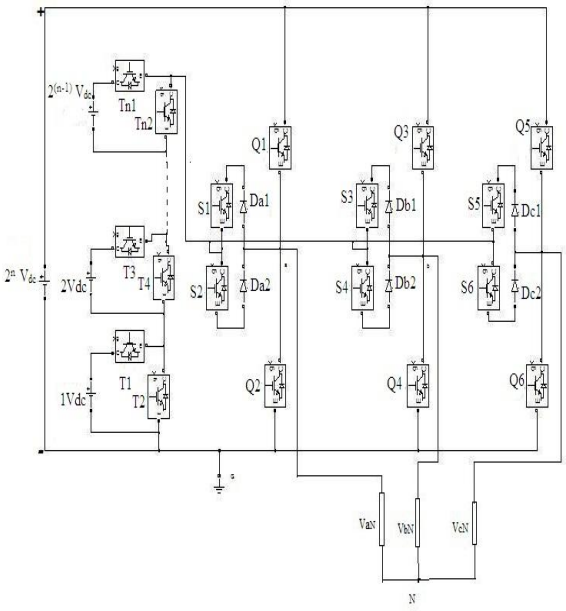


**Fig:2 Circuit diagram of the proposed three-phase *N*-level multilevel inverter (third method).**

3)By making a binary (power of 2) relationship between the dc supplies of the CHB structure as follows:

$$V_{dc1}=2^{(0)}\ V_{dc}$$
$$V_{dc2}=2^{(1)}\ V_{dc}\ \ 2^{j}$$
$$V_{dcn}=2^{(n-1)}\ V_{dc}$$
$$V_{fix} = (N\text{-}1)V_{dc} = \left[1+\sum_{j=1}^{n} 2^{j}-1\right] V_{dc} =2^{n}\ V_{dc}$$
$$N=1+2^{n}$$
$$M=6(N\text{-}1)$$

Table IV illustrates some characteristics of the proposed methods.

**Table-IV**
**Comparison of the maximum number of voltage levels with the required value of DC voltage supplies among the proposed methods.**

| Number of cells | 1st method | | | 2nd method | | | 3rd method | | |
|---|---|---|---|---|---|---|---|---|---|
| n | N | M | Vfix | N | M | Vfix | N | M | Vfix |
| 2 | 4 | 18 | 3Vdc | 5 | 24 | 4Vdc | 5 | 24 | 4Vdc |
| 3 | 5 | 24 | 4Vdc | 8 | 42 | 7Vdc | 9 | 48 | 8Vdc |
| 4 | 6 | 30 | 5Vdc | 12 | 66 | 11Vdc | 17 | 96 | 16Vdc |
| 5 | 7 | 36 | 6Vdc | 17 | 96 | 16Vdc | 33 | 192 | 32Vdc |
| 6 | 8 | 42 | 7Vdc | 23 | 132 | 22Vdc | 65 | 384 | 64Vdc |

Based on the comparison carried among the proposed methods, the following are some observations.

1) Comparing to the second and third methods, the first method has a high modularity degree since the symmetric structure of CHB makes use of equal dc voltage supplies. This method helps the proposed inverter to reach all maximum number of voltage levels (4, 5, 6, 7, 8,. . .,*N*).

2) Since the second and third methods use the asymmetrical structure of CHB, the proposed inverter can reach the required output voltage and the maximum number of voltage levels such as 5, 8, 9, 12, 17,. . . with less number of dc voltage supplies and power electronic components.

## IV. Comparison Study

In order to investigate the capability of the suggested configuration, the proposed inverter is compared with different types of multilevel inverters such as NPC, FC, and CHB. It is evident that the suggested three-phase N-level multi-level inverter can considerably minimize the required number of power components. For the same number of output voltage levels ($N \geq 4$), Table V explains the required number of dc voltage supplies, switches, clamping diodes, control signals, and balancing capacitors of the proposed *N*-level inverter compared with three existing inverters NPC, FC, and CHB. As shown in Fig. 8, it can be noticed that nearly more than two-thirds of number of switches can be counted out as *N* increases. For instance, at the same number of voltage levels $N = 17$, and compared with the existing multilevel inverters which require 96 switches, the required number of switches for the proposed inverter is less since it requires 42 switches based on the first method, 22 switches based on the second method, and 20 switches based on the third method. On the other hand, it is well known that the voltage and current ratings of the power components have an effect on the cost and realization of the multilevel inverter. Assuming that all power components have an equal current rating which is the rated current of the load (*IL*), the voltage ratings of these components depend on the magnitude of dc voltage supplies, voltage stress, and structure of the inverter. Considering that all inverters have the same input dc link which equals.

**Table-V**
**Comparison of the proposed N-level inverter with the existing inverters**

| Converter type | NPC | FC | CHB | Proposed | | |
|---|---|---|---|---|---|---|
| | | | | 1st method | 2nd method | 3rd method |
| Switches | 6(N-1) | 6(N-1) | 6(N-1) | 2(N-1)+10 | $\sqrt{8N-15}$ +11 | $2\log_2$(N-1)+12 |
| Gate drivers | 6(N-1) | 6(N-1) | 6(N-1) | 2(N-1)+7 | $\sqrt{8N-15}$ +8 | $2\log_2$(N-1)+9 |
| Diodes | 6(N-1) | 6(N-1) | 6(N-1) | 2(N-1)+10 | $\sqrt{8N-15}$ +11 | $2\log_2$(N-1)+12 |
| Clamping diodes | 6(N-2) | 0 | 0 | 0 | 0 | 0 |
| DC supplies | N-1 | N-1 | 3(N-1)/2 | N-1 | 1+ [($\sqrt{8N-15}$-1)/2] | 1+$\log_2$(N-1) |
| Clamping capacitors | 0 | 3(N-2) | 0 | 0 | 0 | 0 |
| Control Signals | 6(N-1) | 6(N-1) | 6(N-1) | 2(N-1)+7 | $\sqrt{8N-15}$ +8 | $2\log_2$(N-1)+9 |

**Table-VI**
**Proposed and the existing topologies rating requirements per level-N**

| Proposed inverter | Main Bridge Q1-Q6 $D_{a1}$- $D_{c2}$ | Bidirectional switches S1 to S6 D1 to D6 | Cascaded Half Bridge Switches $T_{11}$ to $T_{N2}$ | | | converter type | NPC | FC | CHB |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1st method | 2nd method | 3rd method | Switches voltage rating | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ |
| Component voltage rating | $(N-1)V_{dc}$ | $(N-2)V_{dc}$ | $V_{dc}$ | $nV_{dc}$ | $2^{(n-1)}V_{dc}$ | clamping diode voltage rating | $V_{dc}$ | 0 | 0 |
| | | | | | | Clamping capacitor voltage rating | 0 | $V_{dc}$ | 0 |
| Active component current | $I_L$ | $I_L$ | $I_L$ | $I_L$ | $I_L$ | Active component current | $I_L$ | $I_L$ | $I_L$ |

(*N*–1) *V*dc, Table VI illustrates the rating requirements for the proposed inverter comparing with the rating requirements for the existing inverters. It is observed that the inverter employs switching devices with high voltage rating. That results in high cost per-switch. Since the topology is introduced with reduced number of switches, gate driver circuit, diodes and no clamping capacitors are involved, the semiconductor devices expenses are considerably recovered.

## V. Simulation Results

To ensure the feasibility of the proposed topology, the inverter was implemented the inverter shown in Fig. 3 was tested under $V_{dc}$ = 75 V in the first cell, $2V_{dc}$=150V in the second cell and $4V_{dc}$ = 300V. The magnitude of the fixed dc supply is determined as $V_{fix}$=$8V_{dc}$=600V. Fixed three-phase series resistive–inductive load (23Ω–3 mH/Phase) in star connection was used.

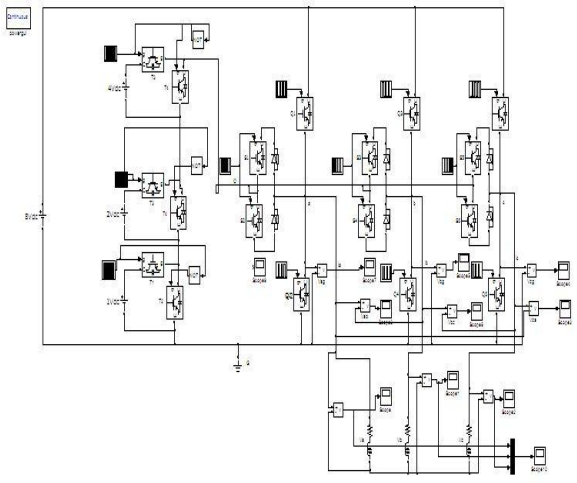

**Fig .3.Simulink model of the proposed three-phase nine-level multilevel inverter.**

The generation principle of the switching gate signals depends on time duration presented in Table II, where the time duration of a cycle of the output waveform (*t* = 1/50 = 0.02 s) is divided into 48 equal time periods:$t_1$=$t_2$=. . . =$t_{48}$ = 0.02/48 s. During each period, the proposed inverter' switches are turned ON/OFF following the switching sequence illustrated in Table II.

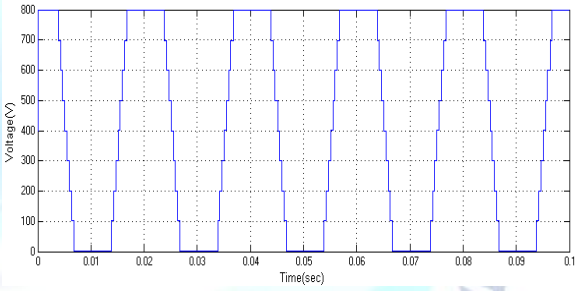


**Fig .4.Simulation output Vag, of proposed nine-level inverter.**

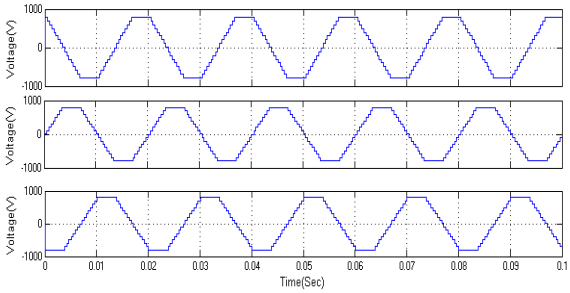


**Fig.5.Simulation output Vab, Vbc and Vca of proposed nine level inverter.**

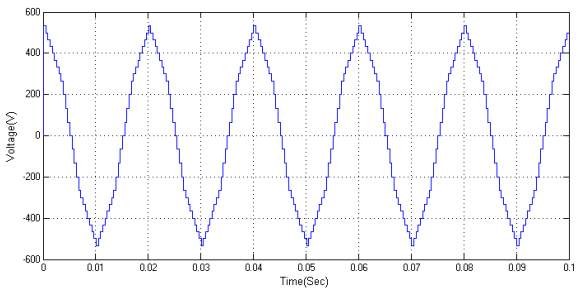


**Fig.6.Simulated waveforms of Van.**

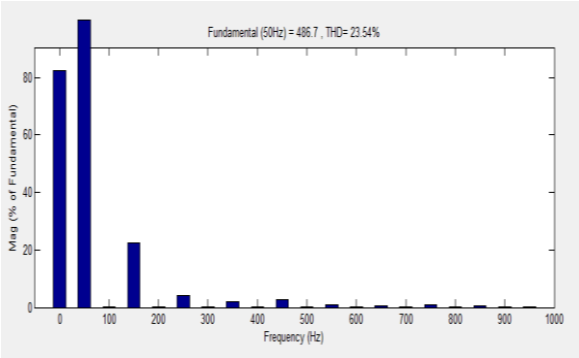


**Fig.7.Total Harmonic Distortion of 9 level phase voltage shows 23.54%.**

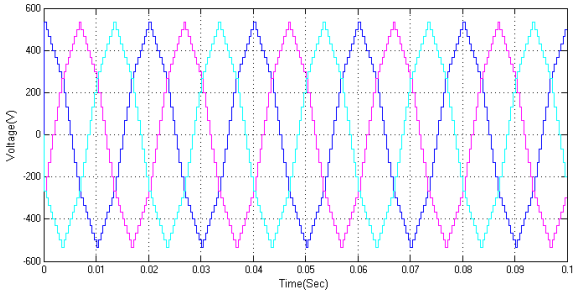


**Fig.8.Three phase output voltage of five level inverter**

Fig.4 depicts the inverter line-to-ground voltage *V*ag . It is clear that the controller manages to generate the appropriate switching gate signals that lead the inverter to output the desired wave-form with five voltage steps. The inverter line-to-line voltages *V*ab, *V*bc, and *V*ca waveforms with nine levels and the inverter line–to-neutral voltages *V*aN, *V*bN, and *V*cN waveforms with 25 levels are shown in Fig.8 , respectively. Due to the symmetry attained in the inverter output line-to-line voltage, all even harmonics components are nearly eliminated.

The value of THD% for the inverter line-to-line output voltage is shown in Fig.7

However, *V*dc took the maximum value of 75 V. Since *V*fix = 8*V*dc and during the testing the maximum dc value was supplied from *V*fix that increased up to 600 V, the inverter efficiency can be calculated based on the measured data as follows:

$$\eta\% = \frac{Pout}{Pin} \times 100$$

where *P*in and *P*out are the inverter input and output power, respectively.

## VI. Conclusion

A new topology of the three-phase nine-level multilevel inverter was introduced. The suggested configuration was obtained from reduced number of power electronic components. Therefore, the proposed topology results in reduction of installation area and cost. Moreover, the proposed configuration was extended to N-level with different methods. Furthermore, the method employed to determine the magnitudes of the dc voltage supplies was well executed. In order to verify the performance of the proposed multilevel inverter, the proposed configuration was simulated. The obtained simulation results met the desired output. Hence, subsequent work in the future may include an extension to higher level with other suggested methods.

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