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Analysis of 7-Level Cascaded & MLDCLI with Sinusoidal PWM & Modified Reference PWM Control Methods

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ABSTRACT

Multilevel inverter offers several advantages compare to the conventional three phase bridge inverter in terms of lower dv/dt stresses, lower electromagnetic compatibility and better THD features. The primary use of DC to AC conversion & speed control of machines also voltage controller and reduce the harmonics in the levels of inverter by using cascade multilevel inverter. This paper presents a comparison of cascaded and multilevel dc link inverter (MLDCLI) Using only a DC power source and capacitors. A MLDCLI can be constructed by the series connection half and full bridge cells each having its own DC source .A multilevel voltage source inverter can be formed by connecting an MLDCL with a single bridge inverter. The MLDCL provides a DC voltage with the shape of a staircase with or without pulse width modulation (PWM) to the bridge inverter, which in turn alternates the polarity to produce an AC voltage. compared with the cascaded multilevel inverter, The MLDCLI can significantly reduce the switch count as the number of voltage levels increases beyond five for a given number of voltage levels , m , the required number of active switches is 2(m -1) for the existing multilevel inverter but is m+3 for the MLDCL inverters.

This paper presents the performance of a seven level cascaded multilevel inverter &MLDCLI Based on a sinusoidalPWM and modified Reference PWM control techniques. Performance analysis is made based on the results of simulation study conducted on the operation of the cascaded & MLDCLI using MATLAB/ SIMULINK. The performance parameters chosen in the work include the waveform pattern harmonic spectrum, fundamental value & total harmonic distortion (THD) of the three phase cascaded H-Bridge MLI & MLDCLI.

I. INTRODUCTION

Power electronics has gone through intense technological evolution during the last three decades. It is a branch of electrical engineering that is concerned with the conversion and control of electrical power for various applications such as industrial, commercial, residential, and aerospace environments. . The utility system usually generates, transmits, and distributes power at a fixed frequency (50 or 60Hz), and fixed voltage is maintained at the consumers terminal. Some residential and industrial applications such as adjustable speed AC drives, induction heating, stand by air craft power supplies, UPS for computers needs three phase adjustable AC power source with controllable frequency and voltage. A power electronics system interfaces between the utility system and industrial loads to satisfy this need. For which we need new types of semiconductor power devices such as IGBT's (with voltage rating as high as 3.3KV and current rating 100A) and IGCT's (4.6 KV and 300A) with attractive switching characteristics and high power handling capacity. As a result of this evolution, today most of these industrial and residential loads are connected to the AC power line through cost effective power converters circuits which enhance the overall efficiency, performance and reliability. Among all the modern power electronics converters, the voltage source inverters (VSI) is the.

II. MULTILEVEL INVERTER

This passage has the aim to introduce to the general principle of multilevel behavior. The leg of a 2-level converter is represented in Figure 1(a) in which the semiconductor switches have been substituted with an ideal switch. The voltage output can assume only two values: 0 or E. Considering Figure.1(b), the voltage output of a

3-level inverter leg can assume three values: 0 , E or 2E . In Figure 1(c) a generalized m-level inverter leg is presented. Even in this circuit, the semiconductor switches have been substituted with an ideal switch which can provide n different voltage levels to the output. In this short explanation some simplifications have been introduced. In particular, it is considered that the DC voltage sources have the same value and are series connected. In practice there are no such limits, then the voltage levels can be different.This introduces a further possibility which can beuseful in multiphase inverters, as it will be shown in the following.

A three-phase inverter composed by m-level legs will be considered for the analysis. Obviously the number of phase-to-neutral voltage output levels is m. The number k of the line-to-line voltage levels is given by

K = 2m-1

Considering a star connected load, the number *p* of phase voltage levels is given by.

P = 2k-1

For example, considering a 5-level inverter leg, it is possible to obtain 9 line-to-line voltage level (4 negative levels, 4 positive levels and 0) and 17 phase voltage levels.

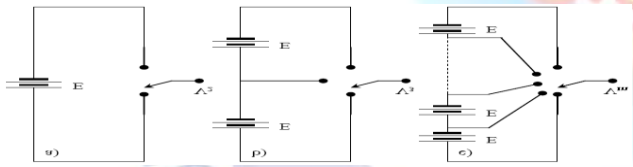

Fig.1:-Multilevel concept for (a) two level (b) three level and (c) m- level

Higher the number of levels gives better quality of output voltage which is generated by a greater number of steps with a better approximation of a sinusoidal wave. So, increasing the number of levels gives a benefit to the harmonic distortion of the generated voltage, but a more complex control system is required, when compared to the 2-level inverter.

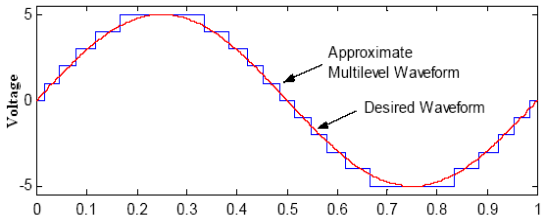

Fig.2:- Example multilevel sinusoidal approximation using 11-levels.

Figure 2 illustrates an example multilevel waveform. Using multiple levels the multilevel inverter can yield operating characteristics such as high voltages, high power levels, and high efficiency without use of transformers. The multilevel inverter combines individual DC sources at specified times to yield a sinusoidal resemblance; by using more steps to synthesize the sinusoidal waveform, the waveform approaches the desired sinusoid and the total harmonic distortion approaches zero.

III. Comparison of Multilevel Inverters

Table compares the power component requirements per phase leg among the three multilevel voltage source inverter mentioned above. Table shows that the number of main switches and main diodes, needed by the inverters to achieve the same number of voltage levels, is the same. Clamping diodes do not need in flying-capacitor and cascaded-inverter configuration, while balancing capacitors do not need in diode-clamped and cascaded-inverter configuration. Implicitly, the multilevel converter using cascaded-inverters requires the least number of components.

Another advantage of cascaded-inverter is circuit layout flexibility. Modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors. The number of output voltage levels can be easily adjusted by adding or removing the full-bridge cells.

Table.1:- comparison of multilevel inverters

Converter Type	Diode clamped	Flying capacitor	Cascaded Inverter	MLDCLI
Main Switching devices	(m-1)*2	(m-1)*2	(m-1)*2	m+3
Main diodes	(m-1)*2	(m-1)*2	(m-1)*2	m+3
Clamping diodes	(m-1)* (m-2	0	0	0
Dc bus capacitors	(m-1)	(m-1)	(m-1)/2	(m-1)/2
Balancing capacitors	0	(m-1)* (m-2)/2	0	0

IV. Cascaded Multilevel Inverter

The last structure introduced in this thesis is a multilevel inverter, which uses cascaded inverters with separate dc sources (SDCSs). The general function of this multilevel inverter is the same as that of the other two previous inverters. The multilevel inverter using cascaded-inverter with SDCSs synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from either batteries, fuel cells, or solar

cells. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new inverter can avoid extra clamping diodes or voltage balancing capacitors.

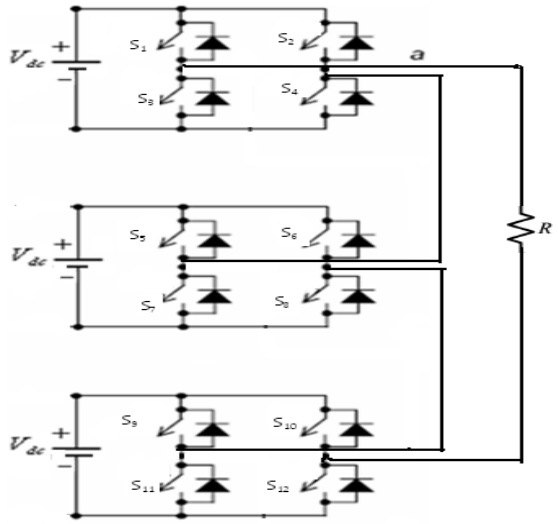

Fig.3:-7-level cascaded Multi level Inverter

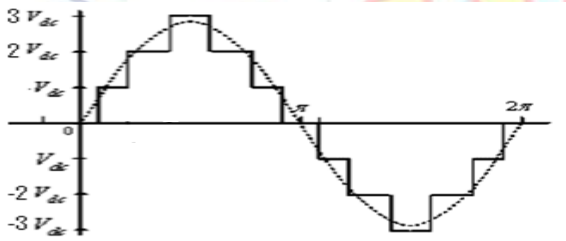

Fig.4:- output wave form of 7 level cascaded inverter

In the case of seven level cascaded the ac output voltage at each level can be obtained in the same as in normal 2 level manner. The AC terminal voltages of different level inverters are connected in series. By different Combinations of the six switchesS1,S4,S5,S8,S9,and S12 each inverter level can generate four different voltage outputs Vdc,2Vdc,3Vdc , and zero as shown in figure. The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. In this topology, the number of outputphase voltage levels is defined bym = 2s+1, where s is the number of dc sources.

least number of components considering there are no extra clamping diodes or voltage balancing capacitors.

Table 2: Switching sequence for singlephase7 level cascaded inverter

O/P voltage	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0vdc	1	0	1	0	1	0	1	0	1	0	1	0
Vdc	1	0	0	1	0	0	1	1	0	0	1	1
2vdc	1	0	0	1	0	0	1	1	1	0	0	1
3vdc	1	0	0	1	1	0	0	1	1	0	0	1
-vdc	0	1	1	0	1	1	0	0	1	1	0	0
-2vdc	0	1	1	0	0	1	1	0	1	1	0	0
-3vdc	0	1	1	0	0	1	1	0	0	1	1	0

Switchingredundancyforinnervoltagelevelsispossible becausethephase voltage output is the sum of each bridge's output.

V. MULTILEVEL DC LINK INVERTER TOPOLOGY

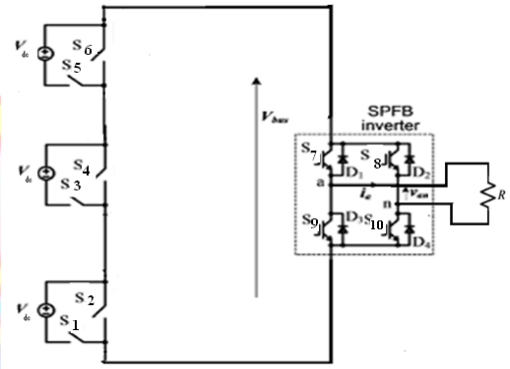

Fig 5: Multi level DC link Seven level inverter

Table 3: Switching sequence for singlephase 7 level MLDCL inverter

O/P voltage	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S 12
0vdc	0	0	0	0	0	0	0	0	0	0	0	0
1vdc	1	0	0	1	0	1	1	0	0	1	0	0
2vdc	0	1	1	0	1	0	1	0	0	1	1	1
3vdc	1	0	1	0	1	0	1	0	0	1	0	1
-1vdc	1	0	0	1	0	1	0	1	1	0	0	0
-2vdc	0	1	1	0	1	0	0	1	1	0	1	1
-3vdc	1	0	1	0	1	0	0	1	1	0	0	1

The proposed single-phase seven-level MLDCL inverter involves various steps of Operations The configuration and the principle of operation of the proposed inverter is given Compared with the existing multilevel inverters, the new MLDCL inverters can significantly reduce the switch count as well as the no of gate drivers as the no of voltage levels increases. For a given no of voltage levels m,

Operations Structure

Table 2: Switching sequen

the new inverter requires m+3 active switches, roughly half of the no of switches, clamping diodes, and voltage-splitting capacitors in the diode clamped configuration or clamping capacitors in the flying capacitor configuration. Simulation and experimental results are included to verify the operating principle of the proposed MLDCL inverters.

VI. Simulation Results

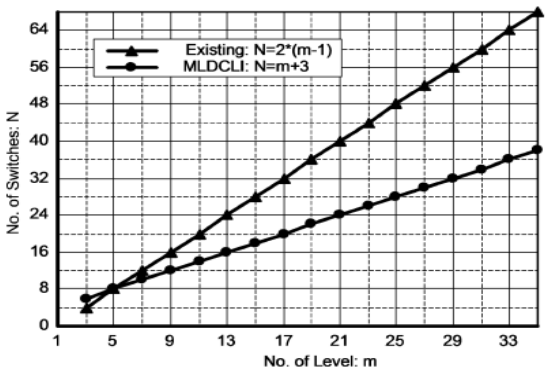

Fig 6: Comparison between cascaded and multilevel dc-link inverter.

From the previous discussions, it is demonstrated that the proposed MLDCL inverters can significantly reduce the component count. Compared with their existing counter parts for a given number of output voltage levels m. It can be seen that roughly half the number of the components can be eliminated as m increases.

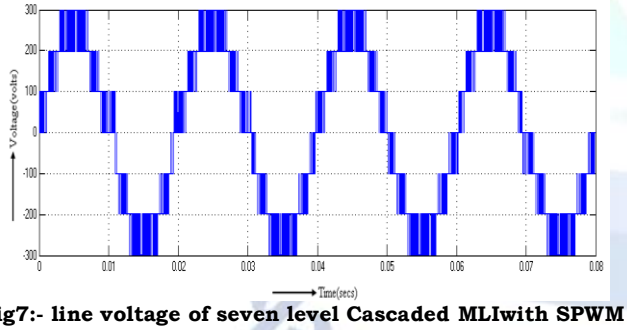

Fig7:- line voltage of seven level Cascaded MLIwith SPWM

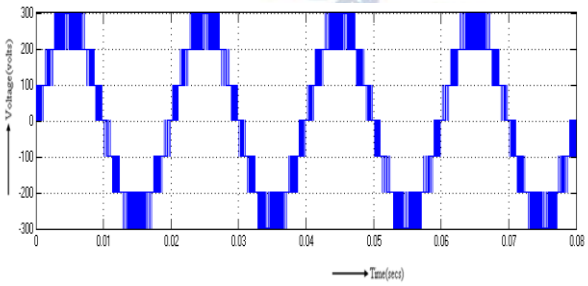

Fig8:- line voltage of seven level Cascaded MLI with Modified reference PWM

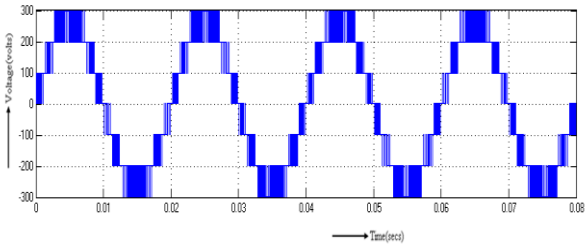

Fig9:- line voltage of seven level MLDCLI With SPWM

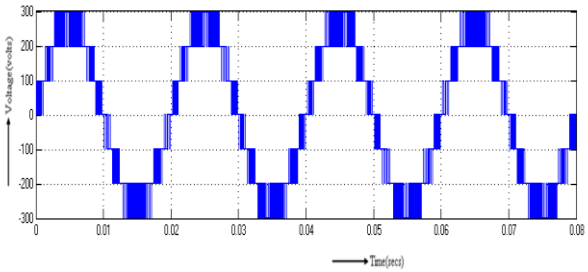

Fig10:-line voltage of seven level MLDCLI With Modified reference PWM

PWM technique	Cascaded 7LI		Multilevel DCL 7LI	
	Fundamental O/P Voltage(V)	THD (%)	Fundamental O/PVoltage(V)	THD (%)
S PWM	253.4	23.13	268.4	22.01
Modified Reference PWM	258.1	22.17	**274.1**	**20.64**

Table.4:- Comparison of 1-phase cascaded seven level Inverter and multilevel DC linkseven level inverter.

VII. Conclusion

A summary of THD and fundamental output voltage for various multilevel inverter topologies with their control strategies are presented. i.e, 7-Level Cascaded inverter and 7-level D.C link inverters were simulated for SPWM and modified SVPWM with triangular carriers. And it is concluded that 7-level dc-link inverter with a modified Reference PWM with triangular carriers has given good fundamental output voltage with less THD .

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