

Implementation of High Speed & Area Efficient Modified Booth Recoder for Efficient Design of the Add-Multiply Operator using VHDL

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ABSTRACT

Many communication applications require multifaceted arithmetic operation are used in many digital signal processing (DSP) relevance. Mainly in the reduction of multiplier power and area consumption it can play an important role in high performance of any digital indication processing system. within this paper, mainly centre of attention on optimizing and increased performance by reduction in power consumption in propose of the fused Add-Multiply (FAM) operator. This implements a new technique by straight recoding of sum two numbers in Modified Booth (MB) form. In this paper implemented a new and efficient structured technique by straight recoding of sum of two numbers by considering existing modified booth (MB) technique. The new technique is implemented by three new dissimilar schemes by integrating them within existing FAM plans. The performance of the proposed three different schemes with the implementation of new model carry select adder (K-adders) gives reduction in conditions of critical delay, hardware complication and power utilization while comparing with the existing AM design.

KEYWORDS: Carry Select Adder9 (K-adder)), Modified Booth (MB), Add-Multiply (AM) operation

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I. INTRODUCTION

In several design Digital Signal Processing (DSP) appliance multiplier plays an significant role. The DSP arrangement uses in modern electronics and make extensive use of custom accelerators for multimedia, communication etc., In the transverse filter, Fast Fourier transform (FFT), implementation of recursive and discrete Fourier transforms, the multiplier is used in their implementation. The performance of DSP arrangement is individually precious by propose concerning the structural design of arithmetic units. In the ground of arithmetic optimization the recent research activities have shown that the

invent of arithmetic mechanism combining operations which share data and which gives significant performance improvements. Based on the observation that an addition can often be subsequent to a multiplication.

While introducing the multiply-accumulator (MAC) and multiply-add (MAD) units leading to high efficient implementations of DSP algorithms when compared to the conventional ones, which use only primitive resources. To optimize the performance of the MAC operations in reduction of area, critical delay and power consumption more number of architectures has been proposed. The most of the DSP applications are used Add-Multiply (AM) operations when compared with

MAC/MAD operations. The MAC/MAD operation performs the multiplication on given inputs and then the result is given to the adder unit. Simply multiplication then addition is processed. In case of Add-Multiply (AM) unit, firstly the inputs are added and then the output of adder is pushing to the input of a multiplier.

The AM unit increases the significant area and critical path delay and power consumption of the circuit when compared with the MAC/MAD unit. Fusion techniques are employed supported on the direct recoding of the sum of two numbers into its modified booth (MB) form to reduce the design of AM operators. Thus the carry propagate adder of the conventional AM design is eliminated resulting in increases performance of the system. A new signed bit MB Recoder which transforms redundant binary inputs to their MB recoding form. A special expansion of the pre-processing step of the Recoder is needed in order to handle operands in carry save representation. In this proposes a two stage Recoder which converts a number in carry put away form to its MB representation. The first step transforms the carry save form of the input number into signed number form which is after that recoded inside the second phase so that it matches the form that the MB digits request. This technique has been used for the design of high performance flexible coprocessor architectures targeting the computationally intensive DSP applications.

In the recoding of a redundant input from its carry keep form to the corresponding borrow set aside form keeping the critical pathway of multiplication operation fixed. When compared to the conventional AM, the direct recoding of the summation of two numbers during its MB form leads to more resourceful performance of the Fused Add Multiply (FAM) component, existing recoding schemes are based on complex multiplications in bit level, which are implemented by dedicated circuits at gate level. In this paper, focuses on efficient design of FAM operator, targeting the optimization of the recoding method for direct determining of the MB form of the sum of two numbers. Specifically in this propose a new recoding technique which decreases critical path delay and reduces power consumption.

During conventional design the multiplicand is formed by adding the inputs A and B, the adder inserts significant delay and this leads to increases in area, power consumption and critical delay. In the proposed design the sum is directly recoded as the MB digit and improves in power consumption,

area and delay in existing intend. In order to be apply either in signed (in 2's complement representation) or unsigned numbers, which comprise of odd or even number of bits the proposed KS-MB algorithm is structured, simple and can be easily modified. In this proposed KSMB approach the three alternative schemes are analyzed using conventional and signed bit half adders (HA's) and Full adders (FA's) as basic building blocks for that proposed KSMB algorithm.

The presentation of the planned KS-MB is appraised by three alternative schemes by comparing with state-of-the-art recoding techniques. The critical path delay, power estimation has been used to provide accurate measurements are estimated regarding various bit-widths of input numbers. Regarding various bit-widths of the input numbers, the industrial tools for RTL synthesis and power estimation have been used to provide accurate measurements of area utilization, critical path delay and power dissipation. For large range of frequencies, the adoption of the proposed recoding technique delivers optimized solution for FAM design enabling the targeted operation to be timing functional. Under the same timing constraints the proposed FAM design deliver improvements in both area occupation and power consumption. The remaining of the paper is organised while in the coming sections we discuss about motivation and present technical background for the implementation of FAM design and the proposed KS-MB recoding scheme is presented and experimental evaluation are given and then clearly identifying the advantages of the proposed KS-MB schemes with respect to critical delay and power dissipation and last section concludes the paper.

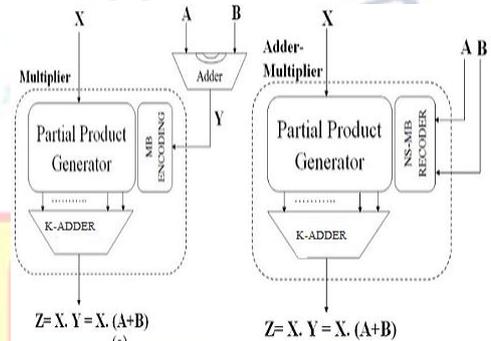
II. LITERATURE SURVEY

This paper mainly focuses on AM units which realize the process $Z = X \cdot (A+B)$. The addition operation is performed on the inputs A and B by using adder and then input X and the adder output i.e., figure $Y = A+B$ are determined to a multiplier within charge to acquire the result (Z) within the conventional design of AM operator (Fig 1(a)). In order to decrease the delay conventional AM design is eliminated resulting in increases performance of the system. A new signed bit MB Recoder which transforms redundant binary inputs to their MB recoding form. A special expansion of the pre-processing step of the Recoder is needed in order to handle operands in carry save representation.

In this we proposes a two stage Recoder which converts a number in carry put away form to its MB representation. The first step transforms the carry save form of the input number into signed number form which is after that recoded inside the second phase so that it matches the form that the MB digits request. This technique has been used for the design of high performance flexible coprocessor architectures targeting the computationally intensive DSP applications. In the recoding of a redundant input from its carry keep form to the corresponding borrow set aside form keeping the critical pathway of multiplication operation fixed. When compared to the conventional AM, the direct recoding of the summation of two numbers during its MB form leads to more resourceful performance of the Fused Add Multiply (FAM) component, existing recoding schemes are based on complex multiplications in bit level, which are implemented by dedicated circuits at gate level. In this paper, focuses on efficient design of FAM operator, targeting the optimization of the recoding method for direct determining of the MB form of the sum of two numbers. Specifically in this propose a new recoding technique which decreases critical path delay and reduces power consumption.

During conventional design the multiplicand is formed by adding the inputs A and B, the adder inserts significant delay and this leads to increases in area, power consumption and critical delay. In the proposed design the sum is directly recoded as the MB digit and improves in power consumption, area and delay in existing intend. In order to be apply either in signed (in 2's complement representation) or unsigned numbers, which comprise of odd or even number of bits the proposed KS-MB algorithm is structured, simple and can be easily modified. In this proposed KSMB approach the three alternative schemes are analyzed using conventional and signed bit half adders (HA's) and Full adders (FA's) as basic building blocks for that proposed KSMB algorithm. The presentation of the planned KS-MB is appraised by three alternative schemes by comparing with state-of-the-art recoding techniques. The critical path delay, power estimation has been used to provide accurate measurements are estimated regarding various bit-widths of input numbers. Regarding various bit-widths of the input numbers, the industrial tools for RTL synthesis and power estimation have been used to provide accurate measurements of area utilization, critical path delay and power dissipation.

For large range of frequencies, the adoption of the proposed recoding technique delivers optimized solution for FAM design enabling the targeted operation to be timing functional. Under the same timing constraints the proposed FAM design deliver improvements in both area occupation and power consumption. The remaining of the paper is organised while in the coming sections we discuss about motivation and present technical background for the implementation of FAM design and the proposed KS-MB recoding scheme is presented and experimental evaluation are given and then clearly identifying the advantages of the proposed KS-MB schemes with respect to critical delay and power dissipation and last section concludes the paper.



Review of the Modified Booth Form: Modified Booth (MB) is a extensive form used in multiplication. The MB encoding uses redundant signed digit radix-4 programming method. The essential benefit of this method is that it decreases the amount of partial products by half in multiplication process comparing to any other radix-2 representation. Let us judge the multiplication of 2's complement statistics X and Y with every number consisting of $n=2k$ spot.

The multiplicand Y can be correspond to in MB form as Digits $\{-2, -1, 0, +1, +2\}$, $0 < j < k-1$, communicate to the three successive bits with one bit extend beyond and allowing for to $n-1 = 0$. the table I shows how the MB digits are formed by summarizing the MB encoding technique. Each figure is symbolize by three bits given name s, one and two. The sign spot (s) represents the number sign either negative (s=1) or optimistic (s=0). Signal one representing the complete value of a numeral is equal to 1 (one=1) or not (one=0). sign two representing the complete value of a number is equal to 2 (two=1) or not (two=0). By means of these three signals (s, one, two) the MB digit is formed and it's represented by following equation

TABLE I
MODIFIED BOOTH ENCODING TABLE

Binary			y_j^{ms}	MB Encoding			Input Carry c_{in}
Y_{2j-1}	Y_{2j}	Y_{2j+1}		Sign= s_j	x 1=one $_j$	x 2=two $_j$	
0	0	0	0	0	0	0	
0	0	1	+1	0	1	0	
0	1	0	+1	0	1	0	
0	1	1	+2	0	0	1	
1	0	0	-2	1	0	1	
1	0	1	-1	1	1	0	
1	1	0	-1	1	1	0	
1	1	1	0	1	0	0	

(a) Boolean equations:
 $one_j = y_{2j-1} \oplus y_{2j}$
 $two_j = (y_{2j-1} \oplus y_{2j}) \cdot one_j$
 $s_j = y_{2j+1}$

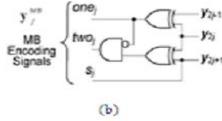
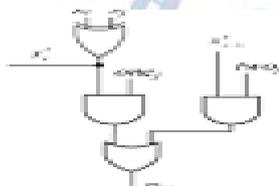


Fig. 2. (a) Boolean equations and (b) gate-level

Fig 2(a) shows the Boolean equations on which the implementation of the MB encoding signals is based (Digits communicate to the three successive bits with one bit extend beyond and allowing for to table I shows how the MB digits are formed by summarizing the MB encoding technique. Each figure is symbolize by three bits given name s, one and two. The sign spot (s) represents the number sign either negative (s=1) or optimistic (s=0). Signal one representing the complete value of a numeral is equal to 1 (one=1) or not (one=0). sign two representing the complete value of a number is equal to 2 (two=1) or not (two=0). By means of these three signals (s, one, two) the MB digit formed and it's represented by following equation Fig 2(a) shows the Boolean equations on which the implementation of the MB encoding signals is based (Fig 2(b)).

1. FAM Implementation:

The proposed FAM design represented in fig 1 (b) The multiplier is a parallel one based on the MB algorithm. Let us consider X,Y, the term $Y = \{ y_{n-1} y_{n-2} \dots y_1 y_0 \}_2$'s is prearranged stand on the MB algorithm and multiply with $X = \{ x_{n-1} x_{n-2} \dots x_1 x_0 \}_2$'s. Mutually X and Y consists of $n=2k$ bits and in 2's complement form. Equation (4) explains the production of the k partial commodities. The partial product is generated and is stand on the subsequently logical appearance while fig (3) demonstrate its execution at gate intensity



2. SCG Unit of the BEC-Based CSLA (K-ADER)

As shown in Fig. 2, the RCA calculates n-bit sum s_0 and c_0 out corresponding to $c_{in} = 0$. The BEC unit receives s_0 and c_0 out from the RCA and generates (n + 1)-bit excess-1 code. The most significant bit (MSB) of BEC represents c_1 out, in

which n least significant bits (LSBs) represent s_1 . The logic expressions

$$s_0^0(i) = A(i) \oplus B(i) \quad c_0^0(i) = A(i) \cdot B(i) \quad (1a)$$

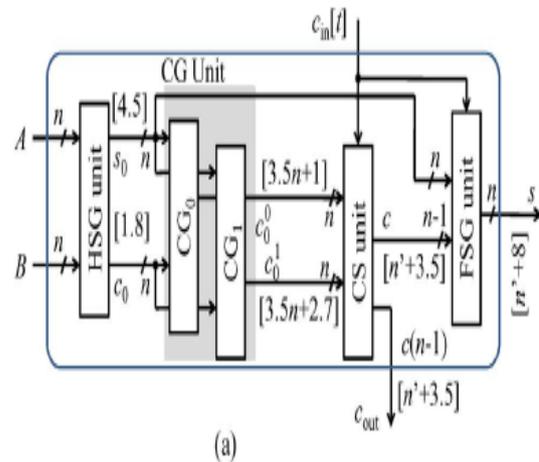
$$s_1^0(i) = s_0^0(i) \oplus c_1^0(i-1) \quad (1b)$$

$$c_1^0(i) = c_0^0(i) + s_0^0(i) \cdot c_1^0(i-1) \quad c_{out}^0 = c_1^0(n-1) \quad (1c)$$

$$s_0^1(i) = A(i) \oplus B(i) \quad c_0^1(i) = A(i) \cdot B(i) \quad (2a)$$

$$s_1^1(i) = s_0^1(i) \oplus c_1^1(i-1) \quad (2b)$$

$$c_1^1(i) = c_0^1(i) + s_0^1(i) \cdot c_1^1(i-1) \quad c_{out}^1 = c_1^1(n-1) \quad (2c)$$



We consider $x-1 = 0$ and $xn = xn-1$ for the working out of the slightest and most considerable bits of partial product respectively. The quantity of ensuing prejudiced products are $\lfloor n/2 \rfloor + 1 = k+1$ in case of $n=2k+1$. Based on sign conservatory of the preliminary 2's complement digit the most significant MB digit is formed. After generation of partial products they are further properly weighted throughout a carry select adder (CSL) and which is prearranged by following equation The output of the carry select adder (CSL) gives the result $Z=X.Y$ as shown in fig 1(b).

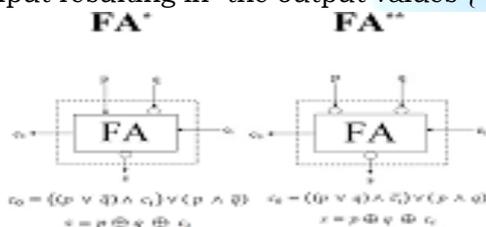
III. NEW SUM TO MODIFIED BOOTH RECODING TECHNIQUES (KS-MB)

Defining signed bit full adders and half adders for structured signed Arithmetic The recoding in this New sum to modified booth Recoder is recorded by considering the two consecutive bits of the input A (a_{2j}, a_{2j+1}) with two consecutive bits of the input B (b_{2j}, b_{2j+1}) into one MB digit. As from eq.(2), the MB digit is formed by including the three bits. The most considerable of them is negatively slanted whereas two least considerable of them have positive weight. Use signed spot calculation in order to make over the two aforementioned couple of bits in MB appearance. In this paper presented a set of bit stage half adders (HA) and Full adders (FA) considering their

inputs and outputs to be signed. Specifically mention here is in this work developed two types of signed Half adders which are referred as HA* and HA** Tables II – IV are their truth tables and their corresponding Boolean equations are represented in fig (4).



The HA* which equipment the relative $2.c-s = p+q$ everywhere the sum s is considered negatively signal (Table II, Fig 4(a)), by considering that p,q are binary contribution and c,s are the outputs (the carry and sum correspondingly) of a HA*. The output gives one of the values {0, +1,+2}. In table III described the dual implementation of HA* which is formed by inverting the signs of all inputs and outputs and consequently, changed the output values to {-2,-1,0}. The relation $2.c-s = -p+q$ shown in fig 4(b) & table IV is implemented by HA** and it shows the operation and schematic of HA**. The result manipulates a negative (p) and a positive (q) input resulting in the output values {-1, 0, +1}.



Also within this paper presented two types of signed FAs (Full Adders) which are presented in table V and VI and fig 5. In the fig 5(a) and 5(b) represents the schematic and shows the relation of FA* and FA** with the conventional FA. The FA* apparatus the relative $2.c_0-s = p - q+c_i$ everywhere the fragment s and q be considered negatively indication (Table V, Fig 5(a)) by assuming p,q and ci are the binary participation and c0 , s be the output carry and sum correspondingly. Output values of FA* are {-1,0,+1,+2} and they are shown in table V (truth table of FA*). In case of FA** equipment the relative $c_0 + s = -p - q+c_i$ (Table VI Fig 5(b)) where p,q are negatively signs. The output values become {-2,-1,0,+1}. The Fig.5 shows the signed FAs implemented using conventional FA with the negative inputs and outputs inverted.

TABLE VI
FA** OPERATION

INPUTS			OUTPUT VALUE	OUTPUTS	
p (-)	q (-)	c _i (+)		c _o (-)	s (+)
0	0	0	0	0	0
0	0	1	+1	0	1
0	1	0	-1	1	1
0	1	1	0	0	0
1	0	0	-1	1	1
1	0	1	0	0	0
1	1	0	-2	1	0
1	1	1	-1	1	1

Output value = -2.c₀+s = -p-q+c₀

Proposed KS-MB Recoding Techniques:

In order to design and explore new three alternative schemes of the New Sum to Modified recoding (KS-MB) technique used both conventional and signed HAs and FAs of section III.A. The three new alternative techniques can be easily either in signed (2's complement representation) or unsigned numbers which consists of odd or even number of bits. In all three schemes considered that both inputs A and B are consist of 2k bits in case of even and (2k+1) bits in case of odd bit-width. Consider the bits a_{2j}, a_{2j+1} and b_{2j}, b_{2j+1} as the inputs of the j-recoding cell to transform the sum of A and B in order to get at its output the three bits that need to form the MB digit according to equation (2).

TABLE II
HA* BASIC OPERATION

INPUTS		OUTPUT VALUE	OUTPUTS	
p (+)	q (+)		c (+)	s (-)
0	0	0	0	0
0	1	+1	1	1
1	0	+1	1	1
1	1	+2	1	0

Output value = 2.c-s = p+q

TABLE III
HA* DUAL OPERATION

INPUTS		OUTPUT VALUE	OUTPUTS	
p (-)	q (-)		c (-)	s (+)
0	0	0	0	0
0	1	-1	1	1
1	0	-1	1	1
1	1	-2	1	0

Output value = -2.c+s = -p-q

TABLE IV
HA** OPERATION

INPUTS		OUTPUT VALUE	OUTPUTS	
p (-)	q (+)		c (+)	s (-)
0	0	0	0	0
0	1	+1	1	1
1	0	-1	0	1
1	1	0	0	0

Output value = 2.c-s = -p+q

TABLE V
FA* OPERATION

INPUTS			OUTPUT VALUE	OUTPUTS	
p (+)	q (-)	C _i (+)		C _o (+)	s (-)
0	0	0	0	0	0
0	0	1	+1	1	1
0	1	0	-1	0	1
0	1	1	0	0	0
1	0	0	+1	1	1
1	0	1	+2	1	0
1	1	0	0	0	0
1	1	1	+1	1	1

Output value = 2.c₀s = p-q+c_i

TABLE VI
FA** OPERATION

INPUTS			OUTPUT VALUE	OUTPUTS	
p (-)	q (-)	C _i (+)		C _o (-)	s (+)
0	0	0	0	0	0
0	0	1	+1	0	1
0	1	0	-1	1	1
0	1	1	0	0	0
1	0	0	-1	1	1
1	0	1	0	0	0
1	1	0	-2	1	0
1	1	1	-1	1	1

Output value = -2.c₀s = -p-q+c_i

KS-MB1 Recoding Scheme:

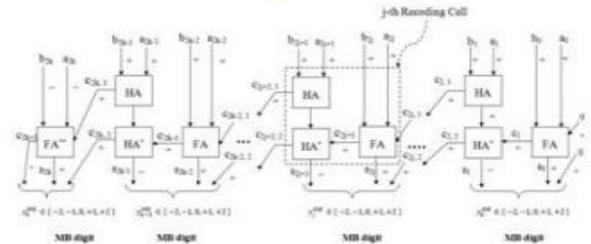
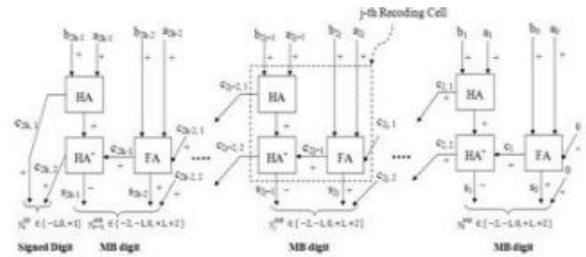
The first scheme in three alternative schemes is demote as the KS-MB1 and is demonstrate in factor in fig (6) for together even (fig 6(a)) and odd (fig 6(b)) bit size of input information. As seen in fig.6 the The programming of the MB digit(0 < j < k-1 of (7) is support on the investigation of section II.B. We consider the early ideals c_{0,1} = 0 along with c_{0,2} =0. The bits s_{2j+1} and s_{2j} are pulling out starting the j recoding cell of fig.6. A conservative FA with inputs a_{2j}, b_{2j} and c_{2j,1} produces the carry) and sum is the output carry of a predictable HA which is component of the (j-1) recoding cell and have the inputs a_{2j-1}, b_{2j-1}. A HA* (Basic operation- Table II, Fig. 4(a)) output sum is s_{2j+1} and which is produced by driving c_{2j+1} and the twisted by a predictable HA with the fragment a_{2j+1}, b_{2j+1} the same as inputs. Within direct to produce the negatively signal sum s_{2j+1}, the HA* is used and its outputs are given by

$$\begin{aligned} c_{2j+2} &= c_{2j+1} \vee (a_{2j+1} \oplus b_{2j+1}) \\ s_{2j+1} &= a_{2j+1} \oplus b_{2j+1} \oplus c_{2j+1} \end{aligned} \quad (8)$$

When we outline the most considerable number (MSD) of the KSMB3 recoding scheme, distinguished the two suitcases, in the first casing the bit width of A and B is even (Fig 6(a)) whereas in the second case both A and B consist of of odd amount of bits (Fig 6(b)) Within casing of even number of bits, the MSD is warning sign digit and is agreed by the relative

$$T_{NSMB1} = T_{HA, Carry} + T_{FA, Carry} + T_{HA^*, Sum} \quad (10)$$

Where THA, Carry and TFA, Carry be the hold-up of determining the output carry of a predictable HA and FA correspondingly delay of structure the sum of a indication HA*

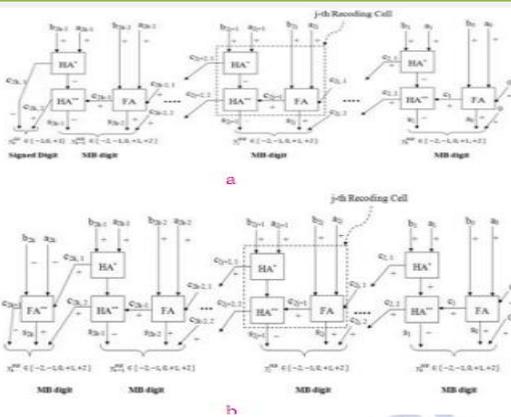


KS-MB2 Recoding Scheme

The second approach execute the projected recoding procedure is NS-MB2. It is demonstrate in detail in fig 7 intended for even (fig 7(a)) as well as odd (fig 7(b)) bit width of input information. Regard as the initial values c_{0,1} =0 and c_{0,2} =0. The digit 0 < j < k-1 stand on s_{2j+1}, s_{2j}, c_{2j,2} according to (7). Again used the predictable FA to construct the carry c_{2j+1} and the sum s_{2j}. A bit c_{2j,1} is the output carry of a HA* (Basic operation-Table II Fig 4(a)), fit in to (j-1) recoding chamber and have input spot a_{2j-1}, b_{2j-1}. The negatively indication bit (s_{2j-1}) formed by a HA** (Table IV, Fig 4(b)) has the inputs c_{2j+1} and the output calculation (ne atively signal) of the HA* of the j recoding cell through the small piece a_{2j+1}, b_{2j+1} as contribution. The carry and sum outputs of the HA** are particular by

$$\begin{aligned} c_{2j+2} &= c_{2j+1} \wedge (a_{2j+1} \oplus b_{2j+1}) \\ s_{2j+1} &= a_{2j+1} \oplus b_{2j+1} \oplus c_{2j+1} \end{aligned} \quad (11)$$

The most significant digit (MSD) for together cases even and odd bit-width of A and B are formed as in



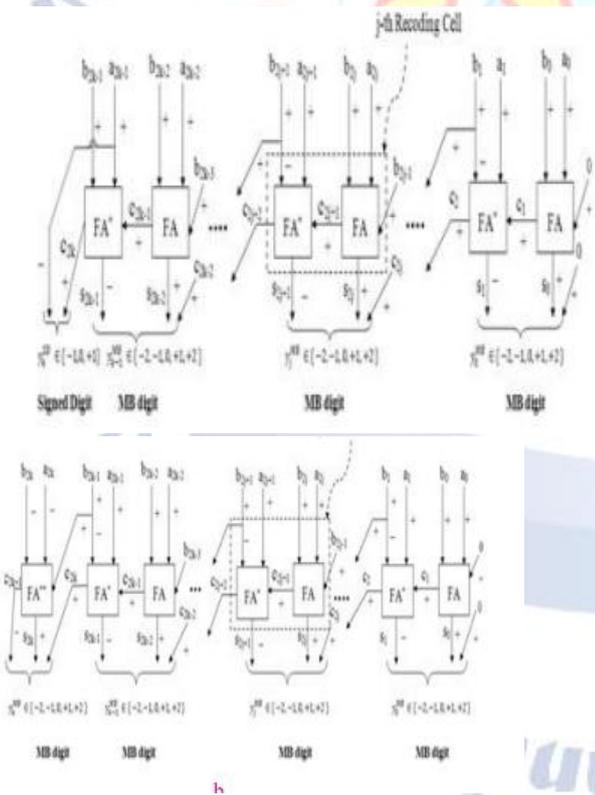
KS-MB2 recoding scheme.

The essential path delay of KS-MB2 recoding scheme is particular by

$$T_{NS-MB2} = T_{HA, Carry} + T_{FA, Carry} + T_{HA^*, Sum} \quad (12)$$

KS-MB3 Recoding Scheme:

The third approach execute the projected recoding method is KSMB3 and is demonstrate in element in fig 8 for together even (Fig. 8 (a)) as well as odd (Fig.8 (b)) bit-width of input information.



The digit, $0 < j < k-1$ are shaped stand on s_{2j+1} , s_{2j} with c_{2j} according to eq (7). Again used the straight FA to construct the carry c_{2j+1} with sum s_{2j} with participation a_{2j} , b_{2j} and b_{2j-1} . Since the bit s_{2j+1} needs to be negatively signal apply FA^* (Table V, Fig 5(a)) with inputs a_{2j+1} , $b_{2j+1}(-)$ and c_{2j-1} which construct the carry c along with the sum s (-)

$$c_{2j+2} = (a_{2j+1} \wedge \overline{b_{2j+1}}) \vee (c_{2j+1} \wedge (a_{2j+1} \vee \overline{b_{2j+1}}))$$

$$s_{2j+1} = a_{2j+1} \oplus b_{2j+1} \oplus c_{2j+1} \quad (13)$$

The MSD is a signed digit and is given by

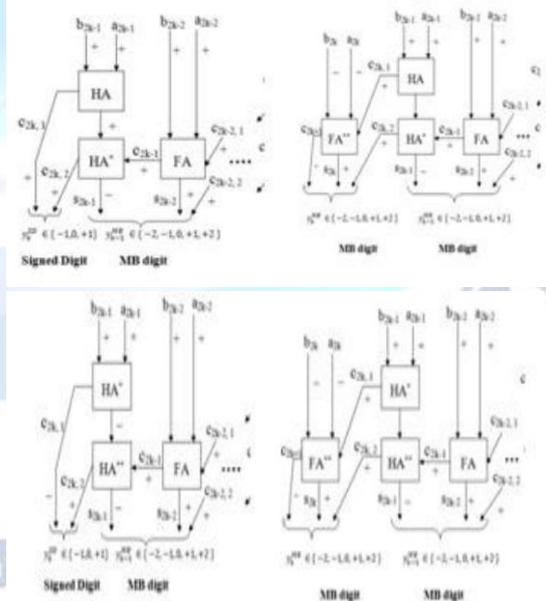
$$SD_{k, even} = -a_{2k-1} + c_{2k} \quad (14)$$

In case that the amount of bits of inputs A with B is odd, the MSD is a MB digit that is formed based on c_{2k+1} , s_{2k} and c_{2k} . The carry c_{2k+1} (-) and the sum s_{2k} are produced by a FA^{**} with inputs a_{2k} (-), b_{2k} (-) and b_{2k-1} (Table VI, Fig 5(b)). The essential path hold-up of NS-MB3 Recoder system is invariable in respect to the input bit measurement and is particular by

$$T_{NS-MB3} = T_{FA, Carry} + T_{FA^*, Sum} \quad (15)$$

Where $T_{FA, Carry}$ is the delay of determining the output carry of a predictable FA and $T_{FA^*, S}$ is the delay of appearance the sum of a signal FA^* Unsigned Input Numbers:

In case that the input numbers A and B are unsigned, their most significant bits are positively signed, Fig 9-11 present the modifications that have to make in all NS-MB schemes for both cases of even (The two most significant digits change) and odd (only the most significant digit change) bit width of A and B regarding signs of the most significant bits A and B. The basic recoding block in all schemes remains unchanged.



IV. PERFORMANCE EVALUATION

The performance of the three proposed recoding schemes in a fused add-multiply operator and they are implemented using VHDL for together cases even as well as odd bit-width of the Recoder's input

information. To evaluate the presentation of the projected KS-MB schemes by evaluate with the active method in terms of critical delay, power consumption is show in table- VII for Even bit width of the inputs. The inputs with odd bit width and their comparison is shown in table-VIII The comparison of power consumption with different techniques is shown in fig. 12 for even bit width as well as for odd bit size is show in fig.13

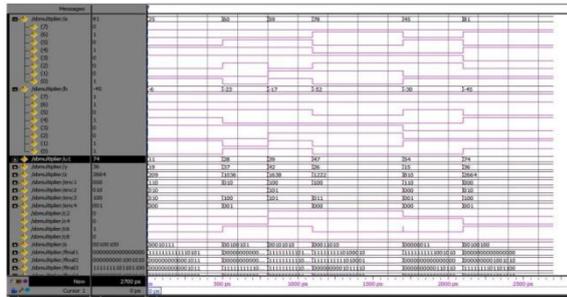


Fig:4 Simulation result of Even Bit Width



Fig 5: Simulation result of odd Bit Width Comparison of delay, power consumption (

S.NO	Method	Time Delay (ns)	Power consumption (mw)	Power Delay Product (pw)
Carry Select Adder				
5	Existing	28.051	130	3646.63
6	S-MB-1	24.764	101	2501.164
7	S-MB-2	24.409	99	2416.491
8	S-MB-3	24.764	99	2451.636
In Built Adder				
9	Existing	17.508	124	2170.992
10	S-MB-1	17.025	100	1702.5
11	S-MB-2	17.025	102	1736.55
12	S-MB-3	16.937	98	1659.826



Fig 6: Graphical comparison

V. CONCLUSION

The design of the fused add-multiply is used to execute the straight recoding of the addition of two information in its modified booth (MB) form. This work focuses on optimizing the invent of the Fused add-multiply (FAM) machinist. In this work explored three new alternative designs of the proposed New sum to modifies booth recoding technique (KS-MB) and compared them with the existing method. The proposed recoding schemes incorporated in FAM designs and they give the performance improvements in conditions of critical delay, power expenditure comparing by way of existing method.

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