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Circulating Current Fault-Tolerant Operation using MMC & PWM Compensation

K.Navatha[1] | N. Ravi Kumar[2]

[1]Associate Professor, Department of EEE, SVR Engineering College, Nandyal, Andhra Pradesh, India
[2]PG Scholar, Department of ECE, SVR Engineering College, Nandyal, Andhra Pradesh, India

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ABSTRACT

The modular multilevel converter (MMC) is an emerging and highly attractive multilevel converter topology for high-voltage and high-power applications. This paper proposes the control method of parallel-connected modular multilevel converters (parallel-MMCs), which assumes that the multiple MMCs are directly connected at both ac and dc sides to effectively enhance the power rating as expected. Two key problems were first solved for the parallel-MMCs under the normal operation conditions: voltage balancing of sub modules and mitigation of circulating currents, where the novel transformed third-order harmonic resonant controller in the synchronous reference frame was employed to mitigate the dominant second-order and fourth-order circulating currents and a sixth-order harmonic resonant controller is used to attenuate the zero-sequence sixth-order circulating current existed in all phase currents per MMC. Considering the high risk of switches fault in the parallel-MMCs, the fault-tolerant operation schemes were then proposed in this paper to address the major concerns of open-circuit and short-circuit switch fault in a sub module, respectively. Carefully controlling the healthy sub modules and the corresponding phase arms, the parallel-MMCs can successfully maintain their balanced capacitor voltages and mitigate the circulating currents with the qualified output waveform obtained. In addition, the parallel configuration of MMCs provides the unique solution for the short-circuit switch fault operation which was seldom discussed in the published literature works with respect to the MMC fault-tolerant operation schemes. MATLAB simulations and the constructed experimental prototype have verified the performance of the proposed control strategy.

KEYWORDS: *Circulating current, fault-tolerant operation, modular multilevel converter (MMC), parallel operation, pulse width modulation (PWM) compensation.*

I. INTRODUCTION

The modular multilevel converter (MMC), which has been originally presented in [1] and [2], is suitable for the applications of high-voltage dc (HVDC) power transmission [3]–[5], adjustable speed motor drives [6], reactive power compensation [7], etc., mainly due to its inherent advantages of the modular structure and the low output voltage/current harmonics. Inside the MMC, every half-bridge converter is considered as a sub module (SM) as shown in Fig. 1, which can be simply cascaded to increase the dc-link voltage to a desired value. However, as the power increases or in other words when the MMC has to handle the high current, a single MMC is increasingly viewed as inappropriate, restricted mainly by the present semiconductor manufacturing technology without any immediate solution. One intuitive solution is to assume the compact integrated parallel-connected

semiconductor switches in each SM, which however need a complicated gate driver to guarantee the simultaneous turning ON/OFF of parallel switches. Besides, assuming a single module with more than two switches connected in parallel would be impractical since the uneven loss distribution, which cannot be simply solved by the gate driver [8],would cause operational failure especially under the high-power highcurrent application conditions. Otherwise, an overdesigned heat dissipation system should be employed, which unfortunately will increase the system cost significantly. Another solution is to assume the parallel-connected setups to equally divide the

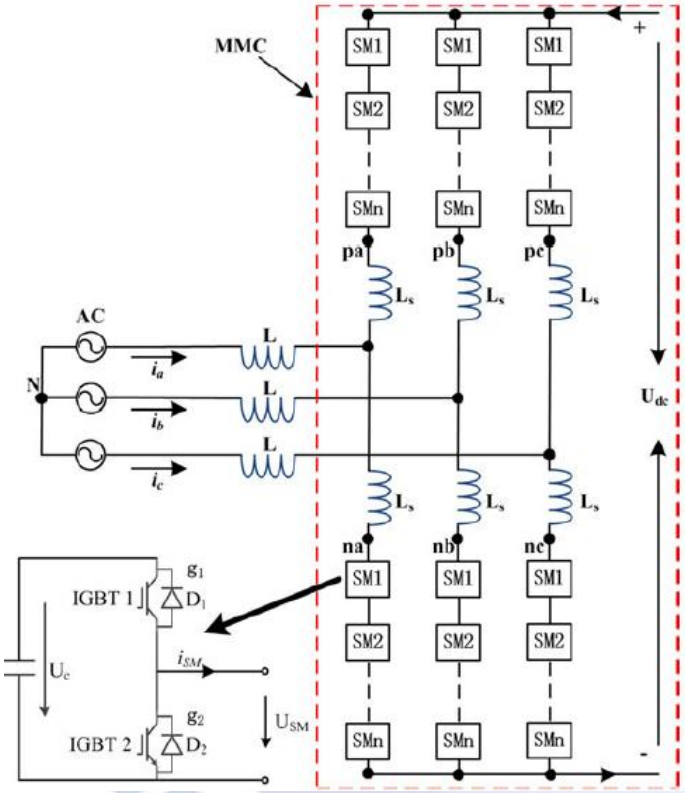

Fig. 1. Topology of the MMC.

Processed current into each setup, where the dc-link and the ac output terminals are directly onnected together. The latter has been widely implemented in two-level converters [9]–[11]. Assuming that the parallel-connected MMCs (parallel-MMCs) will not only effectively increase the power rating as normally expected, but also significantly enhance the operational reliability by both reducing the thermal design burden and providing the unique solutions for semiconductor fault-tolerant operation. However, the parallel configuration of the MMC has been less reported.

In order to successfully implement the parallel-MMCs, two keys issues should be carefully addressed. One is the mitigation of internal and external circulating currents introduced in each phase and between the parallel-MMCs, respectively. Another is the switch fault-tolerant operation scheme without using the expensive redundant hardware to enhance the operational reliability, which is deemed as necessary in a complex multilevel power conversion system. Putting two MMCs in the parallel operation as shown in Fig. 2 would face the situation of cross coupling between the parallel-MMCs because when two MMCs are connected to the same dc bus and ac source/load, the extra zero-sequence circulating current (ZSCC) will result in the unexpected current distortion and the unbalanced load sharing, which would consequently result in the operational failure. Traditionally, in order to avoid this problem, transformers are used in an ac source/load side to isolate the direct current flow. However, the transformer is costly and bulky. As reportedin [12]–[15], the parallel-connected converter can assume a specific control method to attenuate the ZSCC. However, when this method is assumed in the parallel-MMCs, both MMCs should first maintain their dc capacitor voltages of all SMs to be equal. When the voltages of all SMs are balanced, the dc-link voltage can be treated as a constant value when assuming a proper modulation method, thus the parallel-MMCs can be simplified as the two-level converters to attenuate the external ZSCC. Besides, the internal circulating currents should be minimized to reduce the losses. Many papers have reported the internal circulating current control methods [16] , which in principle, control the second-order harmonic current flowing through the phase arms or in addition control the higher order fourth-, sixth-, and eighth-harmonic currents as the added control targets to smooth the internal circulating current, where the well-known resonant controllers are assumed to attenuate each order harmonics. Zhang *et al.* [2] assumed the repetitive controller to attenuate the circulating current. In order to reduce the calculation burden, this paper proposes a transformed third-order harmonic resonant controller in the synchronous reference frame to attenuate both dominant second- and fourth-order circulating harmonics per phase and additionally assumes a generalized sixth-order resonant controller to control the zero-sequence sixth-order circulating harmonic current in all phases per MMC.

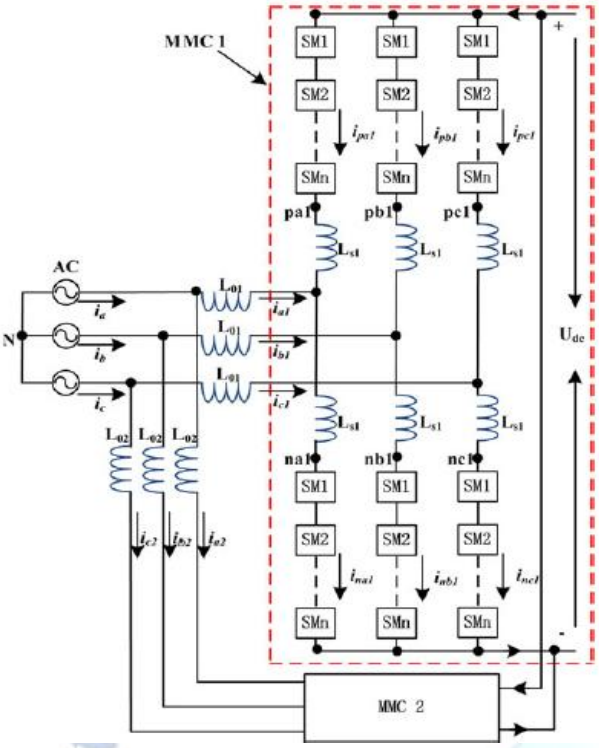

Fig. 2. Topology of the parallel-MMCs.

The high risk of semiconductor switching failure induced by he open-circuit or short-circuit fault in parallel-MMCs cannot be ignored, whose most direct solution is to install a redundant phase-leg connected to the output terminals of normal phase-legs using the triacs the same as that assumed in the low-level power conversion system. Such hardware redundant configuration is expensive and seldom adopted in a high-voltage multilevel converter. The alternative solutions by adjusting the redundant pulse width modulation (PWM) signals in multilevel converters were presented in literature works to compensate the output performance [3]–[6]. The unique configuration of the MMC, however, is not suitable for the onefold PWM compensation scheme under the switch fault-tolerant operation conditions since the dc capacitor in a failure SM has to be inserted in the arm current flowing loop in most of the switching failure cases resulting in the dangerous overvoltage operation. Therefore, before assuming the PWM compensation scheme,the faulty SM should be bypassed first by using an additional bypass switch connected between the output terminals perSMas suggested in [7]. Using the bypass switch can only effectively solve the switch open-circuit failure problem, leaving the case of upper semiconductors (IGBT1 or D1 in Fig. 1) short-circuit failure per SM unsolved. But thanks to the parallel configuration, the parallel-MMCs can ride through all open-circuit and short-circuit semiconductor failure operation conditions using the proposed PWM compensation scheme and the revised control method in this paper without any additional assisted hardware; meanwhile, the proposed control scheme can effectively attenuate all circulating currents as well without sacrificing the output performance.

II. Multilevel Inverter

2.1 Multilevel Concept

This paragraph has the aim to introduce to the general principle of multilevel behaviour. Figure 3.1 helps to understand how multilevel converters work. The leg of a 2-level converter is represented in Figure 3.1a) in which the semiconductor switches have been substituted with an ideal switch. The voltage output can assume only two values: 0 or E . Considering Figure 3.1b), the voltage output of a 3-level inverter leg can assume three values: 0 , E or 2E . In Figure 3.1c) a generalized n-level inverter leg is presented. Even in this circuit, the semiconductor switches have been substituted with an ideal switch which can provide n different voltage levels to the output. In this short explanation some simplifications have been introduced. In particular, it is considered that the DC voltage sources have the same value and are series connected. In practice there are no such limits, then the voltage levels can be different. This introduces a further possibility which can be useful in multiphase inverters, as it will be shown in the following.

A three-phase inverter composed by n-level legs will be considered for the analysis. Obviously the number of phase-to-neutral voltage output levels is n. The number k of the line-to-line voltage levels is given by

$$k = 2n - 1.$$

Considering a star connected load, the number p of phase voltage levels is given by .

$$p = 2k - 1.$$

For example, considering a 5-level inverter leg, it is possible to obtain 9 line-to-line voltage level (3 negative levels, 3 positive levels and 0) and 17 phase voltage levels.

Higher is the number of levels better is the quality of output voltage which is generated by a greater number of steps with a better approximation of a sinusoidal wave. So, increasing the number of levels gives a benefit to the harmonic distortion of the generated voltage, but a more complex control system is required, with the respect to the 2-level inverter.

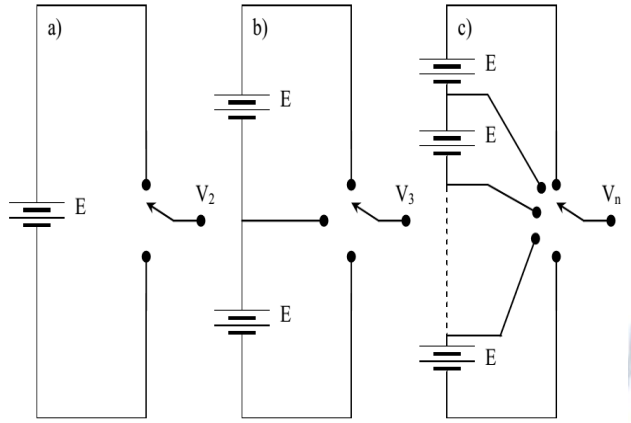

Figure 3.1: Inverter phases. a) 2-level inverter, b) 3-level inverter, c) n-level inverter.

2.2 Multilevel Inverter Performance

The limit of standard three-phase converters is related to the maximum power. Which can be delivered to the load, which is related to the maximum voltage and current of a component. Furthermore, higher is the power of a switch lower is the switching frequency. An initial solution to overcome this problem was to connect several switches in series or in parallel. The series connection of two or more semiconductor devices is really difficult due to the impossibility to perfectly synchronize their commutations. In fact, if one component switches off faster than the others it will blow up because it will be subjected to the entire voltage drop designed for the series. Instead, parallel connection is slightly less complicated because of the property of MOSFETs and more recent IGBTs to increase their internal resistance with the increment of junction temperature. When a component switches on faster than the others, it will conduct a current greater than the current it was designed for. In this way, the component increases its junction temperature and its resistance, so it limits the current which flow through it. This effect makes possible to overcome the problems coming from a delay among gate signals or from differences among real turn on time of the components. Anyway, parallel connection of the switches requires an accurate design of the board.

A modular solution is preferred to increase the power a converter can drive. In this way, a standard three-phase converter is designed with a relatively low power. Then, several converters are paralleled through decoupling inductances to reach the desired power. Even in this system a quite good synchronization among the controls of the converters is required.

Multilevel converters are a viable solution to increase the power with a relatively low stress on the components and with simple control systems. Moreover, multilevel converters present several other advantages. First of all, multilevel converters generate better output waveforms with a lower $\frac{dv}{dt}$ than the standard converters. Then, multilevel converter can increase the power quality due to the great number of levels of the output voltage: in this way, the AC side filter can be reduced, decreasing its costs and losses. Furthermore, multilevel converter can operate with a lower switching frequency than 2-level converters, so the electromagnetic emissions they generate are weaker, making less severe to comply with the standards. Furthermore, multilevel converters can be directly connected to high voltage sources without using transformers; this means a reduction of implementation and costs.

A multilevel inverter is a power-electronic system that generates a desired output voltage by synthesizing several levels of dc input voltages. The main advantages of multilevel inverters are lower cost, higher performance, less electromagnetic interference, and lower harmonic content .The most common multilevel inverter topologies are the diode-clamped, flying-capacitor, and cascaded H-bridge inverters with separate dc voltage sources

2.3 Diode-Clamped

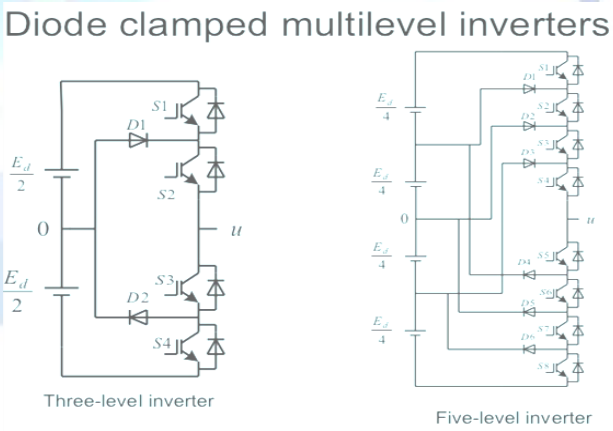

Fig3.2 diode clamped multilevel inverters

2.3.1 Operating Principle

In Figure 3.2, 3-level and 5-level diode-clamped legs are shown; it is easy to extend the scheme to a generic n-level configuration. The DC bus voltage is split in two and four equal steps respectively by capacitor banks. In this way, no extra DC sources are needed with respect to the standard 2-level inverter. The voltage between two switches is clamped through the diodes in the middle of the

structure, called clamping diodes. Considering the 5-level diode-clamped leg, it is possible to note that the number of diodes required to clamp the voltage changes point by point. For instance D_1 is composed only by one diode, instead D_1' is the series of three diodes. This does notmean that the diode series connection is needed in the implementation, but it simply means that the reverse voltage drop born by D_1' is three times the backward voltage drop over D_1 . In the finalimplementation it is allowed to use either one diode with higher blocking capability or three diodes series connected. Anyway, to better understand how a diode-clamped works, it is preferred to use series connected diodes; in this way, the reverse voltage drop of all the diodes is the same and is equal to the voltage fixed by a capacitor. series connected diodes; in this way, the reverse voltage drop of all the diodes is the same and is equal to the voltage fixed by a capacitor.

State	CM voltage	CM voltage V_{DC}~Ipu V_0~0
-1-1-1	-(V_{DC}/2)	-1/2
-1-11	-(1/3)(V_{DC}/2)	-1/6
-11-1	-(1/3)(V_{DC}/2)	-1/6
-111	(1/3)(V_{DC}/2)	+1/6
1-1-1	-(1/3)(V_{DC}/2)	-1/6
1-11	(1/3)(V_{DC}/2)	+1/6
11-1	(1/3)(V_{DC}/2)	+1/6
111	(V_{DC}/2)	+1/2

Table 3.1: 5-level diode-clamped leg relationships between configurations and output voltages.

Making some generalization from Table 3.1 in a n-level diode-clamped leg there are no intra-phase redundant states and n −1 consecutive switches are conducting. Moving the series of conducting switches from the top to the bottom end of the leg, the output voltage decreases from E to 0.

III. IMPLEMENTATION

3.1 Cascaded H-bridge (CHB) topology

The third fundamental multi-level topology is the cascaded H-bridge (CHB). This topology was invented before the other two basic topologies and follows a completely different configuration. Figure 2.4 demonstrates the structure of the 3-level and 5-level CHB inverter.

Each DC source is connected to an H-bridge inverter. The AC outputs of each H-bridge inverters connected in series such that the synthesized voltage waveform is the sum of the inverter outputs.

The name of this topology comes from the modules of H-bridge, or cells, which construct the inverter legs. Tables 2.5 and 2.6 show the allowed switching states for 3-level and 5-level CHB inverter, respectively. As with the other two basic topologies, there are some switching states that should be avoided in order to prevent a shortcut. For instance, s1switches $s1'$and cannot be turned *on* simultaneously because it makes a shortcut of the source. This topology has intra-phase redundant states because the number of allowed configurations is more than the number of required output voltage levels. The reverse voltage drop for this topology is equal tovr=E which is greater than the other two fundamental topologies. Operation of the 3-level CHB inverter is quite easy. When switches (s1,$s2'$) are *on* and (s2,$s1'$) are *off*, the output voltage is +E . Likewise, when switches (s2,$s1'$) are *on* and (s1,$s2'$) are *off*, output voltage is -E. Two redundant exist for the output of 0 . When (s1.s2) are *on* and ($s1's2'$) are *off* or ($s1's2'$) are *on* and (s1.s2) are *off*, output of the inverter is equal to 0. Output voltage for the 5-level CHB inverter can be constructed the same as the 3-level because each cell is able to generate voltage of +E , 0 ,-E and .

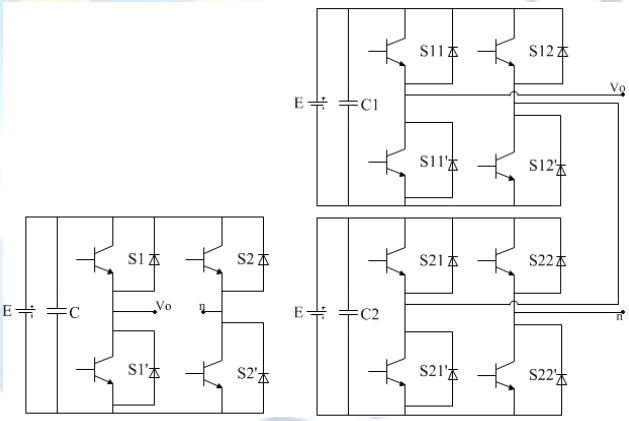

Figure 2.4 Single-phase 3-level and 5-level CHB topology

This topology is limited in that it constructs only an odd number of levels. The first cell generates three levels as each other cell adds two more levels. The topology is very modular and thus easily scalable to higher levels. Each cell has a highly reasonably low cost, as well as desirable reliability which affect the quality of the whole product. In addition, this topology has the advantage of requiring the minimum number of components as compare to the other topologies. Generally, a single-phase n-level CHB inverter consists 2(n-1) of

switches, and (n-1)/2independent DC sources. The primary disadvantage of this inverter is that it requires more than one independent DC source, which is not practical for wind energy applications because only one DC source may be available.

Table 2.5 Switching table for the 3-level CHB topology

Switches				Output Voltage
S1	S2	S1'	S2'	Vo
1	0	0	1	$+E$
1	1	0	0	0
0	0	1	1	0
0	1	1	0	$-E$

Table 2.6 Switching table for the 5-level CHB topology

Switches								Output Voltage
S11	S12	S21	S22	S11'	S12'	S21'	S22'	Vo
1	0	1	0	0	1	0	1	$+E/2$
1	1	1	0	0	0	0	1	$+E/4$
1	0	0	0	0	1	1	1	$+E/4$
1	0	1	1	0	1	0	0	$+E/4$
0	0	1	0	1	1	0	1	$+E/4$
1	1	1	1	0	0	0	0	0
1	1	0	0	0	0	1	1	0
1	0	0	1	0	1	1	0	0
0	1	1	0	1	0	0	1	0
0	0	1	1	1	1	0	0	0
0	0	0	0	1	1	1	1	0
0	1	1	1	1	0	0	0	$-E/4$
0	0	0	1	1	1	1	0	$-E/4$
0	1	0	0	1	0	1	1	$-E/4$
1	1	0	1	0	0	1	0	$-E/4$
0	1	0	1	1	0	1	0	$-E/2$

Indeed, this topology is very helpful for solar or battery-fed applications in which several insulated DC sources are necessary. Additionally, CHB inverters have been suggested for use as the main traction drive electric vehicles (EV) which require several batteries [2], [4].

IV. Conclusion

This paper presents the control methods of parallel-connected MMCs under both normal and switch fault-tolerant operation conditions. In order to reduce the calculation burden meanwhile increase the control accuracy of the internal circulating current suppression method; the resonant controllers are assumed in the synchronous reference frame to suppress the dominant second and fourth-order circulating current harmonics, and a sixth-order resonant controller is employed to suppress the zero-sequence internal circulating current. In addition, when the capacitor voltages are balanced as expected by using the voltage balancing control method, the external ZSCC can then be precisely controlled by treating the MMC as a simple two-level converter. This paper also proposes the fault-tolerant operation schemes as the switch in an SM suffers the open- or short-circuit failure. In principle, the fault-tolerant operation schemes will not influence the output quality by either adjusting the corresponding PWM schemes or the closed-loop control method. MATLAB simulations and the constructed experimental prototype verified the performance of proposed control method.

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