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PV Cell Fed High Step-up DC-DC Converter for PMSM Drive Applications

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ABSTRACT

In this concept novel high step-up dc–dc converter with an active coupled-inductor network is presented for a sustainable energy system. The proposed converter contains two coupled inductors which can be integrated into one magnetic core and two switches. The primary sides of coupled inductors are charged in parallel by the input source, and both the coupled inductors are discharged in series with the input source to achieve the high step-up voltage gain with appropriate duty ratio, respectively. In addition, the passive lossless clamped circuit not only recycles leakage energies of the coupled inductor to improve efficiency but also alleviates large voltage spike to limit the voltage stresses of the main switches. The reverse-recovery problem of the output diode is also alleviated by the leakage inductor and the lower part count is needed; therefore, the power conversion efficiency can be further upgraded. The voltage conversion ratios, the effect of the leakage inductance and the parasitic parameters on the voltage gain are discussed. The voltage stress and current stress on the power devices are illustrated and the comparisons between the proposed converter and other converters are given. The simulation results are presented by using Mat lab/Simulink software.

KEYWORDS: *Active coupled-inductor network (ACLN), high step-up voltage gain dc–dc converter, low voltage stresses.*

I. INTRODUCTION

Advancement in the research of Power Electronic converter is still increasing with the rapid demands in the industry. In search of better efficiency, cost, design flexibility, low harmonics in converters, many converters had been proposed so far. Global energy consumption tends to grow continuously. To satisfy the demand for electric power against a background of the depletion of conventional, fossil resources the renewable energy sources are becoming more popular. The renewable energy sources are considered to be environmentally friendly and harness natural process [1-2].

These sources can provide an alternate cleaner source of energy helps to negate the certain forms of pollution and they are not depleting any source of energy during power generation are also suited to small off grid applications. High gain DC/DC converters are the key part of renewable energy systems. The designing of high gain DC/DC converters is imposed by severe demands. Designers face contradictory constraints such as low cost and high reliability. Generally the applications of high step-up dc-dc converter involves the following requirements as high step-up voltage gain, low input current and output voltage ripple, high current handling capability and

high efficiency. The conventional coupled inductor and switched capacitor based converters perceive high step-up gain because the turns ratio of the coupled inductor can be engage as various control freedom to boost the voltage gain. In the low power gridconnected PV system, the transformer less configuration has become a widespread tendency due to its higher efficiency, smaller size, lighter weight, and lower cost compared with the isolated counterparts [3-5]. However, in the transformer less condition, when the traditional full bridge inverter with unipolar sinusoidal pulse width modulation (SPWM) modulation is adopted, the common mode (CM) ground leakage current may appear on the parasitic capacitor between the PV cell and the ground, which brings out the safety issue and reduces the efficiency of the inverter.

The conventional boost converters are not suitable for the high step-up conversion applications because the duty cycle of the conventional boost converter with high step-up conversion is very large, which results in narrow turn-off period, large current ripple, and high switching losses [6]. In order to achieve large voltage conversion ratio, some switched capacitor based converters were published [7]. With the switched capacitor technology, the conversion ratio of the converter is increased and the voltage stresses of the devices are decreased. Unfortunately, the switched capacitor technique makes the switch suffer high transient current and large conduction losses [8].

The ANC with the switched inductor and switched capacitor is proposed in [9], but the system volume is large and part count is increased greatly under the high voltage conversion gain. The ANC with coupled inductors is further proposed in [10], and the voltage gain is increased by adjusting turns ratio of the coupled inductor and the duty cycle, but the part count is still high. This letter proposes a novel high efficiency high step-up voltage gain converter which combines an active coupled-inductor network (ACLN) and a traditional boost converter with a passive clamping circuit, called the ACLN converter (ACLNC). The proposed converter has the following advantages: high voltage conversion gain, small volume, low voltage stresses on switches, low diodes count, and low conduction losses on switches [11].

The converters require increasing low dc voltage to high dc voltage. The conventional boost converters are able to get high voltage duty ratio the problem is Electro Magnetic Interference and complexity increases. Output voltage controlled with better voltage regulation for various changes in the load conditions. DC-DC converters with coupled inductors can provide high voltage gain, but their efficiency is degraded by the losses associated with leakage inductors. The solution would be the use of transformers to get the preferred voltage conversion ratio similar in forward or fly back converter the dc-isolation is no need for industrial applications. To suppress the high voltage spike on power switch non-dissipative snubber and active clamp circuit is used. The active clamp circuit clamps the surge voltage of switches ad recycles the energy stored in the leakage inductance of the transformer [12]. The leakage energy of the coupling inductor recycles the energy. Without wasting through active clamp, active clamp circuit consists a clamped diode and clamped capacitor. The clamped-voltage dc-dc converter [13] with reduced reverse recovery current and switch-voltage stress.

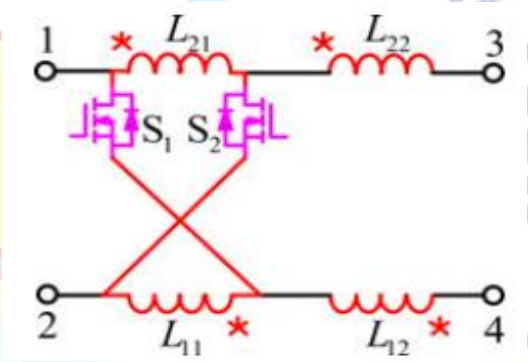

Fig. 1. The active coupled-inductor network (ACLN).

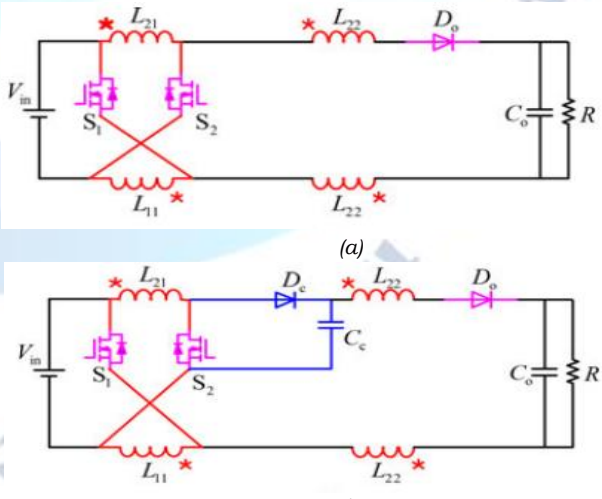

Fig. 2. Proposed high step-up ACLN dc–dc boost converter. (a) ACLNC. (b) ACLNC with a passive lossless clamped circuit.

II. Proposed High Step-up Converter

The proposed converter contains an ACLN which is shown in Fig.1. The ACLN consists of two coupled inductors (L11 and L12, L21 and L22) which have

the same inductance value and two same switches (S1 and S2) which share the same operation signal. By combining the ACLN with the traditional boost converter, the ACLN dc–dc boost converter (ACLNC) is obtained, as shown in Fig. 2(a), in which the output voltage is greatly enhanced. The proposed high step-up converter is constructed by two coupled inductors made up of four windings L11, L12, L21, and L22, two switches S1 and S2, one output diode Do, and one output capacitor Co. The leakage inductance is inevitable in the proposed ACLNC, which results in high voltage spikes, large switching losses, and severe EMI problems. In general, the dissipated RCD circuit can be used for absorbing the leakage inductance, but the losses induced by the RCD circuit are significant and the efficiency is degraded. Therefore, passive lossless clamped circuits are applied here to recycle the leakage energy and to suppress the voltage spikes as shown in Fig. 2(b) [6].

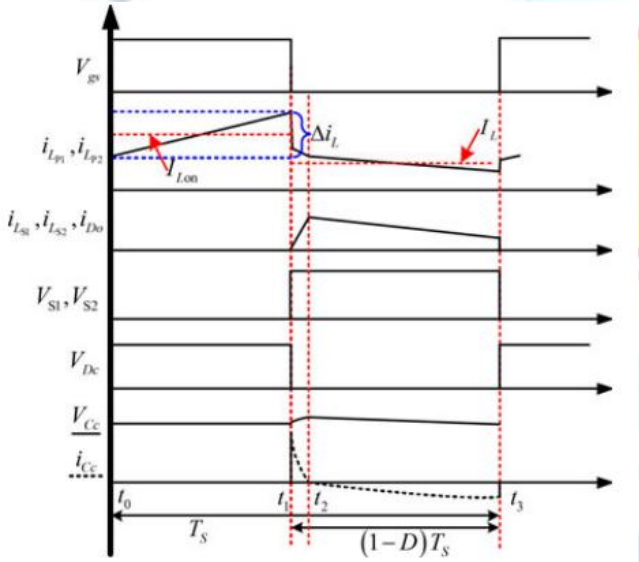

Fig.3. Some typical waveforms of the proposed ACLNC.

III. Basic Operating Principle

Fig.3 briefly illustrates the key waveforms of the proposed ACLNC. Only the operating principle in continuous-conduction mode (CCM) is discussed in this letter. The transient states in operating principle will not be discussed here because the parasitic resistance and the parasitic capacitance of the two active switches and diodes are neglected. Fig. 4(b)–(d) shows the equivalent circuits of the proposed ACLNC under the following assumptions:

1) The capacitors Cc and Co are large enough so that the voltages on them are considered to be constant.

2) The switches and diodes are ideal. In order to clearly show the current flows, the ideal switches take the place of MOSFETs in ON state or OFF state, as shown in Fig. 4(a).

3) The equivalent circuit model of the coupled inductor includes two ideal coupled inductors LPi and LSi and two leakage inductors Lki (i = 1,2).

4) To make the following derivation simple, define K as LP i/(LP i +Lki) and the turns ratio of LP1 to LS1 and LP2 to LS2 is 1 : N (N > 1). LP1, LP2 and LS1, LS2 share the same inductance, respectively.

A. CCM Operation

The three steady operating modes are described as follows.

1)Mode I [t0,t1]: During this time interval, the switches S1 and S2 are turned ON. Diodes Dc and Do are reverse biased. The current-flow path is shown in Fig. 4(b). The primary sides of both coupled inductors are in parallel charged. The currents inductor iLP 1 andiLP 2 are increased linearly. Output capacitor Co provides its energy to the load R. When the switches S1 and S2 are turned OFF at t1, this operating mode ends.

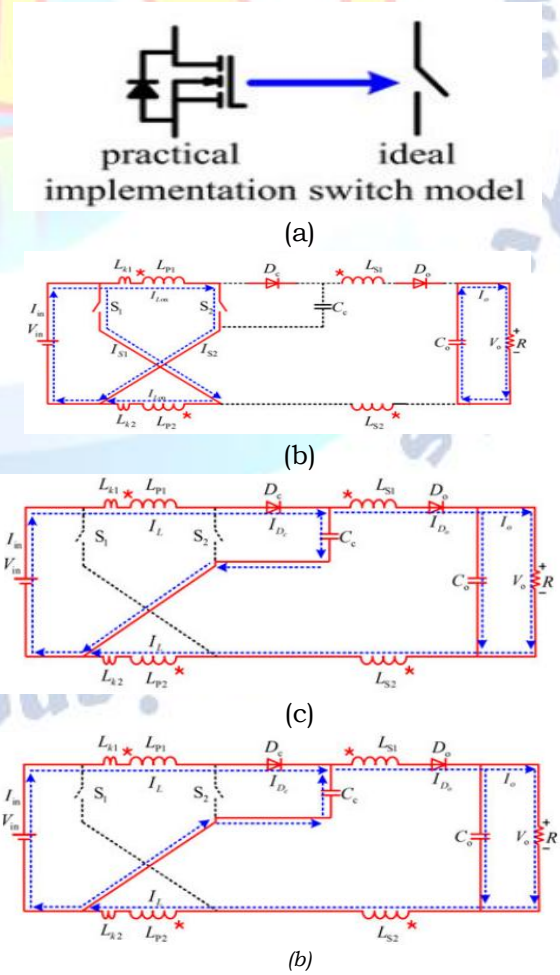

Fig.4. Equivalent circuits of the proposed ACLNC.

Thus, according to the KVL, the voltage equation across coupled inductors is expressed as follows:

$$V_L^I = 2(NK+1)V_{in} \quad (1)$$

where VL represents the voltage on both the coupled inductors.

2)Mode II [t1,t2]: During this time interval, the switches S1 and S2 are turned OFF. Diodes Dc and Do are forward biased. The leakage energy flows into the clamped capacitor Cc. Meanwhile, the dc source Vin and the energies stored in the coupled inductors are transferred to output capacitor Co and the load R. This operating mode is ended when the charging current of clamped capacitor iC c is equal to zero, as shown in Fig. 4(c). The voltage across both coupled inductors can be expressed as

$$V_L^{II} = V_{in} - V_o \quad (2)$$

3) Mode III [t2, t3]: During this time interval, the switches S1 and S2 remain OFF. Diodes Dc and Do are still forward biased. The current-flow path is shown in Fig. 4(d). The clamped capacitor Cc is discharging. Concurrently, the dc source Vin and the energies stored in the coupled inductors are transferred to output capacitor Co and the load R. This operating mode is ended when the switches S1 and S2 are turned ON att3. The voltage across both coupled inductors can be written as

$$V_L^{III} = V_{in} - V_o \quad (3)$$

IV. Circuit Performance Analysis

A. Steady-State Analysis

By applying the volt–second balance principle on coupled inductors, the following equation is formed:

$$\int_{t_0}^{t_1} V_L^I dt + \int_{t_1}^{t_2} V_L^{II} dt + \int_{t_2}^{t_3} V_L^{III} dt = 0 \quad (4)$$

Substituting (1)–(3) into (4) and collecting terms, the voltage gain is obtained as

$$M_{CCM} = (D(2NK+1)+1)/(1-D) \quad (5)$$

By employing the clamp circuits, the voltage strikes caused by the leakage inductance are suppressed and the energy stored in the leakage inductance is recycled to the load. Especially, the reverse-recovery problem of the diodes Do is solved. However, the leakage inductance causes the duty ratio losses. The schematic of the voltage gain versus the duty ratio under various leakage inductance Lk1 and various turns ratio of the coupled inductors. As the turn's ratio increases, the voltage gain of this converter increases. On the contrary, as the leakage inductance increases, the voltage gain of this converter decreases. In order to further clearly show the effect of the leakage inductance, the effect of the leakage inductance and the turns ratio on the voltage conversion gain when the converter operate under D = 0.6. Therefore, some consideration should be made when the leakage inductance is big during the design. When leakage inductance is zero, the ideal voltage gain can be written as

$$M_{CCM} = (D(2N+1)+1)/(1-D) \quad (6)$$

B. Voltage Stresses and Current Stresses on Power Devices

The voltage ripples on the capacitors and the leakage inductances are ignored to simplify the voltage stresses analysis on the components of the proposed converter. The voltage stresses of the main switch S1, S2 and clamped capacitor Cc are given by

$$V_{S1} = V_{S2} = V_{C_c} = V_{in}/(1-D) \quad (7)$$

The voltage stresses on diodes Do and Dc related to the turns ratio and the input voltage can be derived as

$$V_{D_o} = V_{in}(2N+1)/(1-D) \quad (8)$$

$$V_{D_c} = V_{in}/(1-D) \quad (9)$$

The on-state average currents of the output diode Do and clamped diode Dc are calculated as

$$I_{D_o} = I_{D_c} = I_o/(1-D) \quad (10)$$

The root-mean-square (RMS) currents through the switches can be obtained by assuming the inductor current ripples of primary sides of coupled inductors as $\Delta i_L = K_L I_{Lon}$,

$$I_{S1-RMS} = I_{S2-RMS} = \frac{(1+N)\sqrt{D}}{1-D} \cdot \frac{P_o}{V_o}\sqrt{\frac{K_L^2}{12}+1} \quad (11)$$

Where Po is the output power.

C. Comparison with Other Converters

Due to the dual-switch structure, the current ripple is minimized to reduce the conduction loss, the passive component size is reduced, and the power level is increased. In order to clearly demonstrate the circuit advantages of the proposed converter, a detailed comparison is made among the conventional boost converters, boost converter with switching coupled-inductor [Boost-SCL] ultra large gain step-up switched-capacitor dc–dc converter with coupled inductor [USC-CL] a coupled inductor SEPIC converter [CL-SEPIC] passive clamp-mode coupled-inductor boost converters with coupled inductor [CM-Boost-CL] in [6], and the proposed ACLNC are highlighted in Table I.

Some specific variable symbols of all parasitic components are assumed as follows:VD is the forward voltage drop of diodes; rL is the ESR of inductors; rDS is the on-state resistance of the switch; rD represents the forward resistance of diode; and R represents the load. According to the

previous work the theoretical dc gain and efficiency influenced by the parasitic parameters and duty cycle are also obtained in Table. I.

TABLE I

Performance Comparison among Different Converters

Topology	Boost	Boost-SCL	USC-CL	CL-SEPIC	CM-Boost-CL	ACLN(
Active switches	1	1	1	1	1	2
Diodes	1	2	4	2	2	2
Magnetic cores	1	1	1	2	1	1
Voltage gain	$\frac{1}{1-D}$	$\frac{1+ND}{1-D}$	$\frac{C3}{1-D}$	$\frac{(1+N)D}{1-D}$	$\frac{ND+1}{1-D}$	$\frac{C6}{1-D}$
Voltage stress of active switch	$\frac{V_{in}}{1-D}$	$V_{in}\frac{1+ND}{1-D}$	$\frac{V_{in}}{1-D}$	$V_{in}\frac{1+ND}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$
Current stress of active switch	$\frac{I_0}{1-D}$	$\frac{I_0(N+1)}{1-D}$	$\frac{I_0N(D+1)}{D(1-D)}$	$\frac{I_0(D+N)}{1-D}$	$\frac{I_0(N+1}{1-D}$	$\frac{I_0(N+1}{1-D}$
Voltage stress of output diode	$\frac{V_{in}}{1-D}$	$V_{in}\frac{1+ND}{1-D}$	$\frac{NV_{in}}{1-D}$	$V_{in}\frac{1+ND}{1-D}$	$\frac{NV_{in}}{1-D}$	$\frac{(1+2N)V}{1-D}$
Cost	small	medium	medium	medium	small	mediun
Voltage gain with parasitic resistance	$\frac{A1}{B1}$	$\frac{A2}{B2}$	$\frac{A3}{B3}$	$\frac{A4}{B4}$	$\frac{A5}{B5}$	$\frac{A6}{B6}$
Efficiency with parasitic resistance	$\frac{A1(1-D)}{B1}$	$\frac{A2(1-D)}{B2(1+ND)}$	$\frac{A3(1-D)}{B3C3}$	$\frac{A4(1-D)}{B4C4}$	$\frac{A5(1-D)}{B5(ND+1)}$	$\frac{A6(1-D}{B6C6}$

V. Permanent Magnet Synchronous Motor (PMSM)

Permanent magnet synchronous motors (PMSM) are typically used for high-performance and high-efficiency motor drives. High-performance motor control is characterized by smooth rotation over the entire speed range of the motor, full torque control at zero speed, and fast acceleration and deceleration. To achieve such control, vector control techniques are used for PM synchronous motors. The vector control techniques are usually also referred to as field-oriented control (FOC). The basic idea of the vector control algorithm is to decompose a stator current into a magnetic field-generating part and a torque generating part. Both components can be controlled separately after decomposition. Then, the structure of the motor controller (vector control controller) is almost the same as a separately excited DC motor, which simplifies the control of a permanent magnet synchronous motor. Let's start with some basic FOC principles.

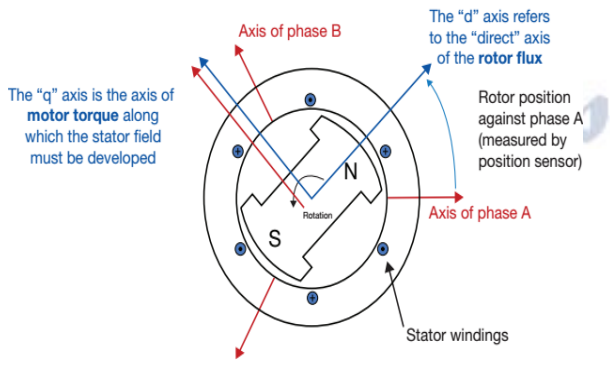

Fig 5 schematic diagram of PMSM drive

A reactance torque of PMSM is generated by an interaction of two magnetic fields (one on the stator and one on the rotor). The stator magnetic field is represented by the magnetic flux/stator current. The magnetic field of the rotor is represented by the magnetic flux of permanent magnets that is constant, except for the field weakening operation. We can imagine those two magnetic fields as two bar magnets, as we know a force, which tries to attract/repel those magnets, is maximal, when they are perpendicular to each other. It means that we want to control stator current in such a way that creates a stator vector perpendicular to rotor magnets. As the rotor spins we must update the stator currents to keep the stator flux vector at 90 degrees to rotor magnets at all times. The reactance torque of an interior PM type PMSM (IPMSM) is as follows, when stator and rotor magnetic fields are perpendicular. Torque=$32pp\lambda_{PM}I_{qs}$ *pp* – Number of pole pairs 1 PM – Magnetic flux of the permanent magnets *I* qs – Amplitude of the current in quadrature axis As shown in the previous equation, reactance torque is proportional to the amplitude of the q-axis current, when magnetic fields are perpendicular. MCUs must regulate the phase stator current magnitude and at the same time in phase/angle, which is not such an easy task as DC motor control.

DC motor control is simple because all controlled quantities are DC values in a steady state and current phase/ angle is controlled by a mechanical commentator. How can we achieve that in PMSM control? DC Values/Angle Control First, we need to know the rotor position. The position is typically related to phase A. We can use an absolute position sensor (e.g., resolver) or a relative position sensor (e.g., encoder) and process called alignment. During the alignment, the rotor is aligned with phase A and we know that phase A is aligned with the direct (flux producing) axis. In this state, the rotor position is set to zero (required voltage in d-axis and rotor position is set to zero, static voltage vector, which causes that rotor attracted by stator magnetic field and to align with them [with direct axis]).

1 Three-phase quantities can transform into equivalent two-phase quantities (stationary reference frame) by Clarke transformation.

2. Then, we transform two-phase quantities into DC quantities by rotor electrical position into DC values (rotating reference frame) by Park transformation. The electrical rotor position is a mechanical rotor position divided by numbers of magnetic pole pairs pp. After a control process we

should generate three-phase AC voltages on motor terminals, so DC values of the required/generated voltage should be transformed by inverse Park/Clarke transformations.

VI. MATLAB/SIMULINK RESULTS

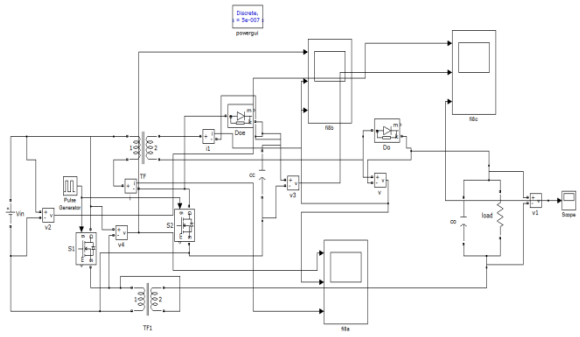

Fig 6 Simulation model of Step-Up DC–DC Converter with an Active Coupled-Inductor

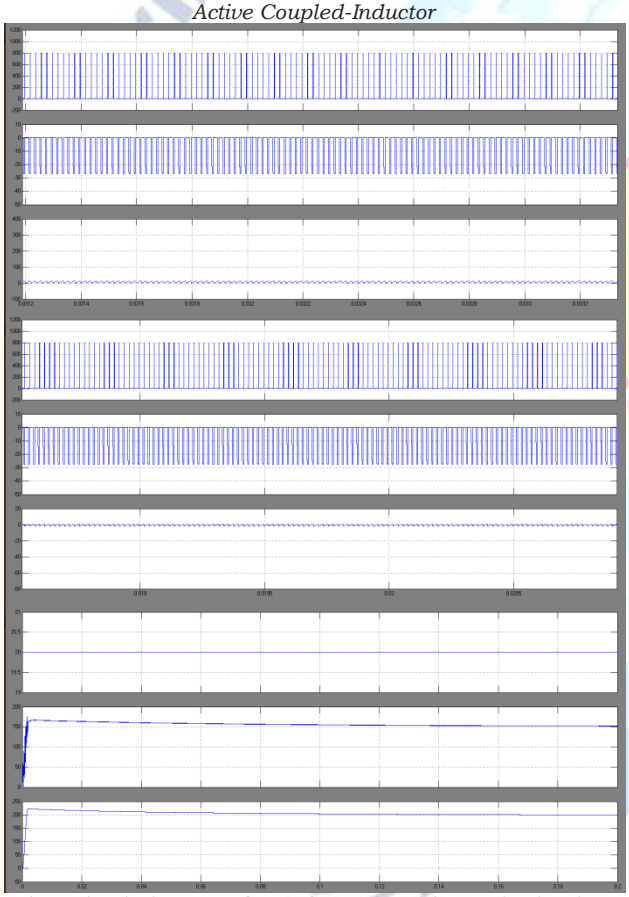

Fig 7 Simulation waveform of ACLNC with passive lossless clamping

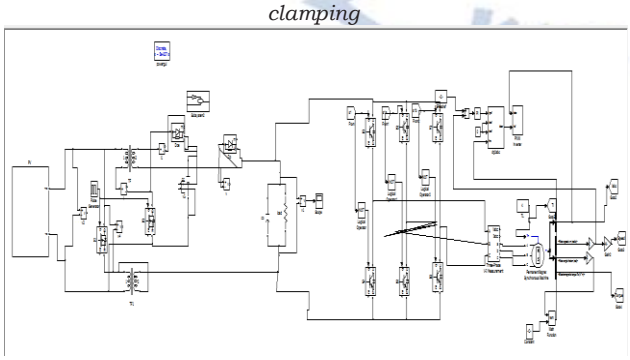

Fig 8 Simulation model of PV high Step-Up DC–DC Converter with an Active Coupled-Inductor connected to PMSM drive

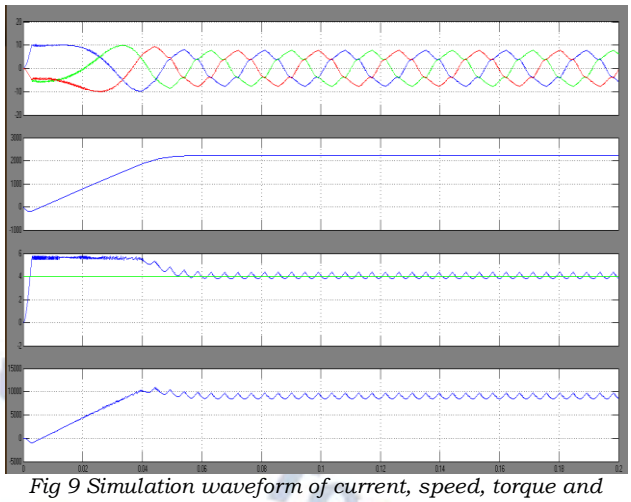

Fig 9 Simulation waveform of current, speed, torque and reference speed

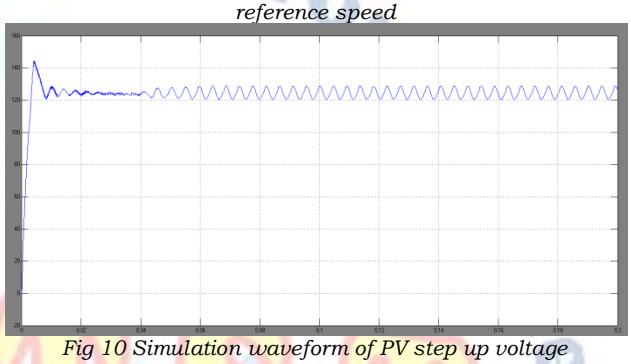

Fig 10 Simulation waveform of PV step up voltage

VII. CONCLUSION

High voltage gain can be achieved with the reduced magnetic size lower part count contributes not only to the lower cost but also to higher power conversion efficiency; low voltage power switches can be selected, which can help to reduce the on-state resistance of the switch and the loss. However, the extensive use of power electronics based equipment with pulse width modulated variable speed drives are increasingly applied in many new industrial applications such as induction motors that require superior performance like low losses and high reliability. The proposed converter has successfully implemented an efficient high step-up conversion through the voltage multiplier module with high efficiency. Leakage energy is recycled and voltage spikes are constrained. Voltage stress on power switch is also lower than output voltage i.e.,400v. The proposed converter has successfully implemented an efficient high step-up conversion through the voltage multiplier module. The interleaved structure reduces the input current ripple and distributes the current through each component. In addition, the lossless passive clamp function recycles the leakage energy and constrains a large voltage spike across the power switch. Meanwhile, the voltage stress on the power switch is restricted and much lower than the

output voltage these all simulation results are tested and verified by usingMATLAB/SIMULINK software.

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