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Fuzzy Logic Controller Based on Voltage Source Converter-HVDC with MMC Topology

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ABSTRACT

This paper presents Modular Multi Level Converters (MMC) are used for high voltage high power DC to AC conversion. The MMCs with increased number of levels offer close to sine wave operation with reduced THD on the AC side. This is a new type of voltage source converter (VSC) topology. The use of this converter in a high-voltage direct current (HVDC) system is called by a MMC-HVDC system. The MMC-HVDC has the advantage in terms of scalability, performance, and efficiency over two-and three-level VSC-HVDC. The proposed HVDC system offers the operational flexibility of VSC based systems in terms of active and reactive power control, in addition to improved ac fault ride-through capability and the unique feature of current-limiting capability during dc side faults. The proposed VSC-HVDC system, in this project assesses its dynamic performance during steady-state and network alternations, including its response to AC and DC side faults. In this project using a fuzzy controller and the proposed topology is implemented in MATLAB/ SIMULINK environment and the simulation results are observed.

KEYWORDS: *HVDC, Modular Multi Level Converter (MMC), Fuzzy logic controller, Voltage Source Converter.*

I. INTRODUCTION

The electricity networks of today increasingly need control and stability at high levels of loading. Increasing the stability through adding more lines is not always an option due to restrictions in right-of-way or limits to acceptable short circuit current. The new HVDC system known as VSC-HVDC, has Voltage Source Converters and Pulse Width Modulation (PWM) at its core, different from current source converters in traditional HVDC [1]. Modular Multi Level Converters (MMC) are suitable for high voltage and high power applications especially useful in the large power transaction systems like HVDC [2]. Modular Multi Level Converters are also useful in static power filters and compensator in power systems. With single DC source if a multi level inverter is opted for then the use of the cascaded H bridge inverter scheme will be ruled out as it need isolated DC sources. The other options for constructing multi level inverters with single DC source will be the diode clamped or the flying capacitor type of multi level inverters [3].

The uneven or unequal distribution of energy sourcing by each level of the converter leads to the uneven charge discharge characteristics and this leads to power quality problems. With the modular multi level inverter the problem of capacitor voltage balancing as that found in the diode clamped inverter is eliminated. Another added feature with the MMC is that any number of MMC units or levels can be easily augmented. In pumping large power into the three phase

AC grid, from a huge DC source like the DC bus of the HVDC system or from that of a large DC power pool derived from large Photo Voltaic farm, the three important factors to be considered are that the terminal voltage is maintained in accordance with the grid, the incoming source should be in compliance with the power quality requirements as applicable to the grid and finally for the maximum utility of the MMC the power fed into the grid from the MMC should happen with unity power factor. As and when the command for real power demand to be met by the MMC is received the controller should govern the MMC in

association with the existing PWM techniques like typical Multi Carrier Sinusoidal PWM or the Space Vector PWM such that the aforesaid power transaction requirements are met with [4].

In the last decade, voltage-source-converter high-voltage dc (VSC-HVDC) transmission systems have evolved from simple two-level converters to neutral-point clamped converters and then to true multilevel converters such as modular converters. This evolution aimed to lower semiconductor losses and increase power-handling capability of VSC-HVDC transmission systems to the level comparable to that of conventional HVDC systems based on thyristor current-source converters, improved ac side waveform quality in order to minimize or eliminate ac filters, reduced voltage stresses on converter transformers, and reduced converter overall cost and footprint. The new HVDC transmission systems based on a voltage-source multilevel converter with ac side cascaded H-bridge cells. The adopted converter has inherent dc fault reverse blocking capability, which can be exploited to improve VSC-HVDC resiliency to dc side faults. With coordination between the HVDC converter station control functions, the dc fault reverse-blocking capability of the converter [4].

This project presents a new HVDC transmission systems based on a voltage-source multilevel converter with fuzzy logic controller. The adopted converter has inherent dc fault reverse blocking capability, which can be exploited to improve VSC-HVDC resiliency to dc side faults. With coordination between the HVDC converter station control functions, the dc fault reverse-blocking capability of the hybrid converter is exploited to achieve the following:

- Eliminate the ac grid contribution to the dc fault, hence minimizing the risk of converter failure due to uncontrolled over current during dc faults;
- Facilitate controlled recovery without interruption of the VSC-HVDC system from dc-side faults without the need for opening ac-side circuit breakers;
- Simplify dc circuit breaker design due to are duration in the magnitude and duration of the dc fault current; and, improve voltage stability of the ac networks as converter reactive power consumption is reduced during dc-side faults.

II. Structure and Principle of a MMC

A. Basic Concept and Structure

Fig. 1 shows MMC concept with controllable voltage source and capacitor. Each of these capacitors with their switches represents one sub module. Each of these sources represents one arm of the converter and the two arms which correspond to one phase are called leg of the converter. These controllable voltage sources have to meet the criterion that their voltage sum always has to match the constant DC link voltage. Therefore, if the value of the voltage source in the upper arm is increased, the voltage source value in the lower arm should be decreased respectively and vice versa.

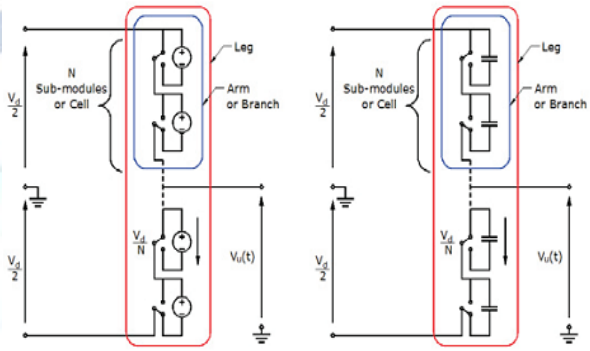

Fig.1. MMC concept with (a) controllable voltage source and (b) capacitors.

The possible switching states of an MMC sub module are when the switch T2 is switched ON, then cell voltage is equal to zero since the capacitor is bypassed. To apply the voltage V_c to the terminals, the switch T1 has to be switched ON, in order to connect the capacitor, Fig. 2. Practically each sub module equipped with the protection switch K1 and a press pack thyristor, K2 is fired during the fault, allowing most of the over current to flow through the thyristors and not through the freewheeling diodes [5].

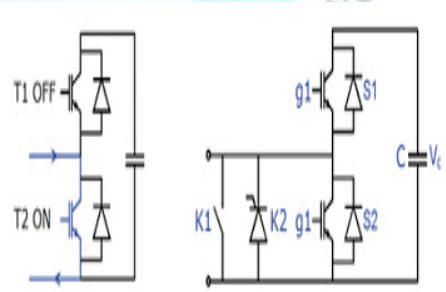

Fig.2. (a) MMC sub module, and (b) practical sub module

The sub module capacitors charges and discharges actively in the converter modulation usually through a specific algorithm to provide constant voltage. However, the capacitor voltages are still not constant, which could result in circulating current due to unequal voltages between the legs. For this reason inductances are also placed in each arm. The single phase MMC

circuit and the respective three phase topology are shown in Fig. 3.

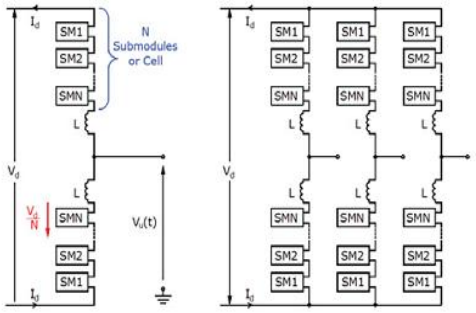

Fig.3. Single phase concept and three phase MMC topology.

B. Averaged Model

Averaged model is developed to make preliminary considerations and have an easier understanding of the MMC system. Each of commutation sub module can be seen as a controlled voltage source as shown in Fig. 1. The structure is composed by a negative and a positive arm each of which is composed by the series of ó sub module with direct modulation shown in Fig. 4.

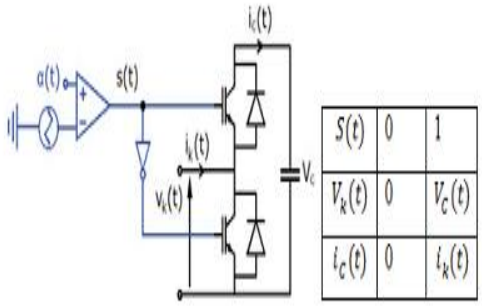

Fig.4. Direct modulation of sub module

By supposing a SPWM modulation with infinity switching frequency, the modulation ratio M and ω_o is the grid frequency. The insertion indexes α in (1) are referred for each branch, the negative and the positive, and are complementary between them.

$$m(t) = M\sin(\omega_o t) \quad ; 0 < M < 1 \tag{1}$$

$$\alpha_1(t) = \frac{1+m(t)}{2} = 1 - \alpha_2(t) \tag{2}$$

In this way the averaged model in Fig. 4 can be extracted in the (3) and (4).

$$V_k(t) = \alpha(t).V_C(t) \tag{3}$$

$$i_C(t) = \alpha(t).i_k(t) \tag{4}$$

C. Mathematical Description

From the equivalent circuit Fig.5, L is the series arm inductor. R denotes the arm losses. V_u is the converter AC output voltage. i_u is the AC output line current. V_d is the DC bus voltage between the positive and negative line. I_d is the DC line current. The arm voltages generated by the cascaded sub modules are expressed as V_n and V_p and the subscript p denotes the lower arm while n denotes the upper arm. From the averaged model, the upper and lower arm voltage can be expresses as:

$$v_{nu}(t) = \frac{1}{2}V_d(1 + M\sin(\omega_0 t)) \tag{5}$$

$$v_{pu}(t) = \frac{1}{2}V_d(1 - M\sin(\omega_0 t)) \tag{6}$$

Because the 2nd harmonic component appears in averaged model simulation results, so the upper and lower arm voltage in (5) and (6) should be rewritten as:

$$v_{nu}(t) = \frac{1}{2}V_d(1 + M\sin(\omega_0 t)) + V_{2f}\sin(2\omega_0 t + \varphi) \tag{7}$$

$$v_{pu}(t) = \frac{1}{2}V_d(1 - M\sin(\omega_0 t)) + V_{2f}\sin(2\omega_0 t + \varphi) \tag{8}$$

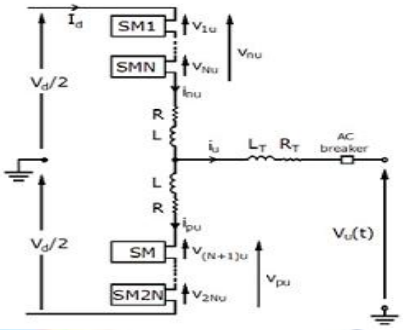

Fig.5. Detailed circuit for single phase of the MMC

Arm currents i_{nu}, i_{pu} and circulating current i_{dif} can be expressed as:

$$i_{nu} = i_{dif} + \frac{i_u}{2} \tag{9}$$

$$i_{pu} = i_{dif} - \frac{i_u}{2} \tag{10}$$

$$i_{dif} = \frac{i_{nu}+i_{pu}}{2} \tag{11}$$

In steady state, the DC line current I_d is supposed to distribute equally among the three phase leg, thus the inner current i_{dif} described in (3) contains one third of the DC line current $I_d/3$ [4]. The arm currents in one phase are described as:

$$i_{nu}(t) = \frac{1}{3}I_d(1 + K\sin(\omega_0 t + \varphi)) \tag{12}$$

$$i_{pu}(t) = \frac{1}{3}I_d(1 - K\sin(\omega_0 t + \varphi)) \tag{13}$$

The 2nd harmonic voltage excites the circulating current through two arm inductors, so the upper

and lower arm current in (12) and (13) should be rewritten as:

$$i_{nu}(t) = \frac{1}{3} I_d (1 + K\sin(\omega_0 t + \varphi)) + I_{2f}\cos(2\omega_0 t + \varphi) \quad (14)$$

$$i_{pu}(t) = \frac{1}{3} I_d (1 - K\sin(\omega_0 t + \varphi)) + I_{2f}\cos(2\omega_0 t + \varphi) \quad (15)$$

D. Dimensioning Arm Inductor and Cell Capacitor

The circulating current suppressing method in [4] gives the parameter of the arm inductor at a given peak value of the 2nd harmonic circulating current as:

$$L = \frac{1}{8\omega_0^2 C V_c}\left(\frac{S}{3I_{2f}} + V_d\right) \quad (16)$$

Where V_c is the nominal voltage capacitor with the nominal value is 2.5 kV, and S is the apparent power of the converter.

The capacitor is selected with a value so that the ripple of the sub module voltages is kept within a range of 10% [5]. To achieve this, the energy stored in each sub module should be in the range of 30–40 kJ/MVA. The sub module capacitance is:

$$C = \frac{2S.E_{MMC}}{6N.{V_C}^2} \quad (17)$$

Where E_{MMC} is the energy stored per megavolt ampere (kJ/MVA) on each converter.

E. Control of a MMC

Common advance method of the MMC HVDC control system, the example in Fig. 6, divides into two categories:

(1) Upper level control system (blue), such as standard VSC control include space vector control strategy which is required to change the current from the present value to the reference value. The current orders to the controller are calculated from preset active and reactive powers and preset AC and DC voltages [5].

(2) Low level control system (red), principally contain circulating current suppression control (CCSC), modulation control method such as nearest level control (NLC), and sub module capacitor balancing algorithm (CBA).

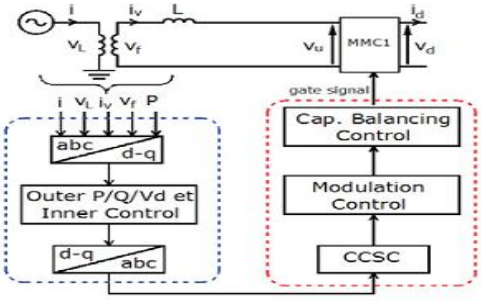

Fig.6. Common MMC HVDC control system.

In this PSIM based fault study, the control of MMC will follow a SPWM control block diagram with basic voltage loop and current loop in [6].

The block diagram of control is depicted in Fig.7. Calculation of the PI controller of voltage loop refers to value of bandwidth 10 to 20 Hz phase margin 60o, and PI controller of current loop refers to the classic value of bandwidth $\frac{f_c}{4}$ to $\frac{f_c}{2}$and phase margin 60°.

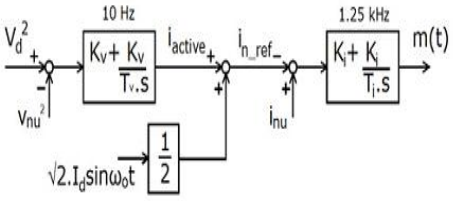

Fig.7. Block diagram of control

In the form of the transfer function of voltage loop at overcrossing frequency (B_{pv}) 10 Hz and current loop at overcrossing frequency (B_{pi}) 1.25 kHz is given by:

$$H_v(s) = k_v.\frac{V_d}{2}.\frac{2}{C}.\frac{1+sT_v}{sT_v} \quad (18)$$

$$H_i(s) = k_i.V_d.\frac{1}{sL}.\frac{1+sT_i}{sT_i} \quad (19)$$

The gains are derived by assuming $sT_v \sim j\omega T_v \gg 1$, and the time constants are derived by considering phase margin that value of $60^0 = \sqrt{3}$. The gains and the time constants are:

$$k_v = \frac{C}{N}\frac{2\pi.Bpv}{V_d} \qquad T_v = \frac{\sqrt{3}}{2\pi.Bpv}$$

$$k_i = L\frac{2\pi.Bpv}{V_d} \qquad T_i = \frac{\sqrt{3}}{2\pi.Bpv} \quad (20)$$

F. Fuzzy Logic Control

L. A. Zadeh presented the first paper on fuzzy set theory in 1965. Since then, a new language was developed to describe the fuzzy properties of reality, which are very difficult and sometime even impossible to be described using conventional methods. Fuzzy set theory has been widely used in the control area with some application to power system [5]. A simple fuzzy logic control is built up by a group of rules based on the human knowledge of system behavior. Matlab/Simulink simulation model is built to study the dynamic behavior of converter. Furthermore, design of fuzzy logic controller can provide desirable both small signal and large signal dynamic performance at same time, which is not possible with linear control technique. Thus, fuzzy logic controller has been potential ability to improve the robustness of compensator.

The basic scheme of a fuzzy logic controller is shown in Fig .8. and consists of four principal components such as: a fuzzy fication interface, which converts input data into suitable linguistic values; a knowledge base, which consists of a data base with the necessary linguistic definitions and the control rule set; a decision-making logic which, simulating a human decision process, infer the fuzzy control action from the knowledge of the control rules and linguistic variable definitions; a de-fuzzification interface which yields non fuzzy control action from an inferred fuzzy control action [10].

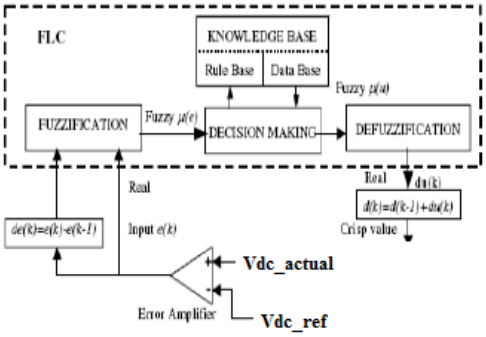

Fig.8. Block diagram of the Fuzzy Logic Controller (FLC) for Proposed Converter.

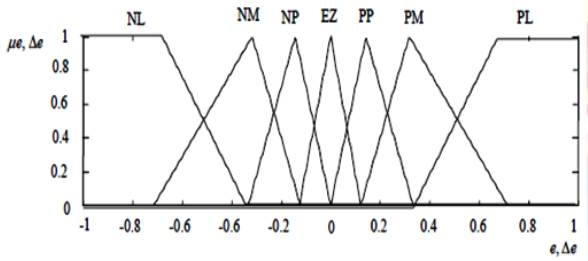

Fig.9. Membership functions for Input, Change in input, Output.

Rule Base: the elements of this rule base table are determined based on the theory that in the transient state, large errors need coarse control, which requires coarse in-put/output variables; in the steady state, small errors need fine control, which requires fine input/output variables. Based on this the elements of the rule table are obtained as shown in Table, with '*Vdc*' and '*Vdc-ref*' as inputs

e / Δe	NL	NM	NS	EZ	PS	PM	PL
NL	NL	NL	NL	NL	NM	NS	EZ
NM	NL	NL	NL	NM	NS	EZ	PS
NS	NL	NL	NM	NS	EZ	PS	PM
EZ	NL	NM	NS	EZ	PS	PM	PL
PS	NM	NS	EZ	PS	PM	PL	PL
PM	NS	EZ	PS	PM	PL	PL	PL
PL	NL	NM	NS	EZ	PS	PM	PL

III. Simulation Results

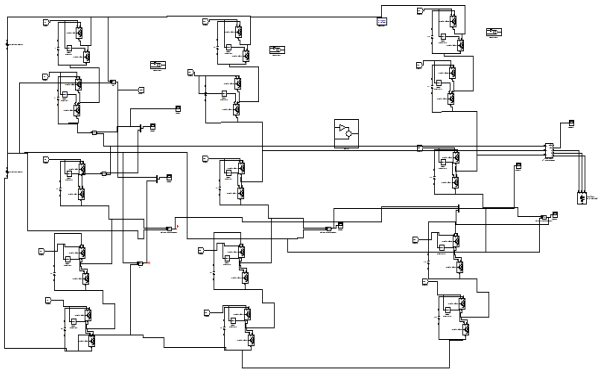

Fig.10 simulation diagram

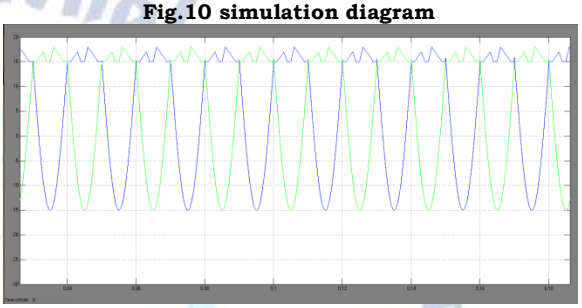

Fig.11 Arm current

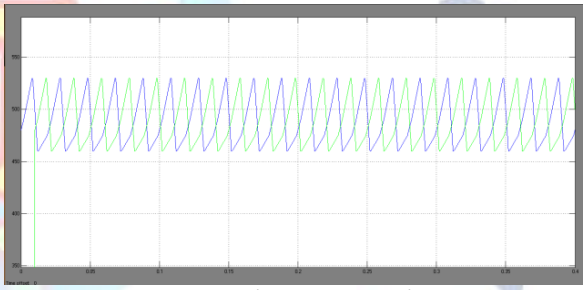

Fig. 12 Total capacitor voltage.

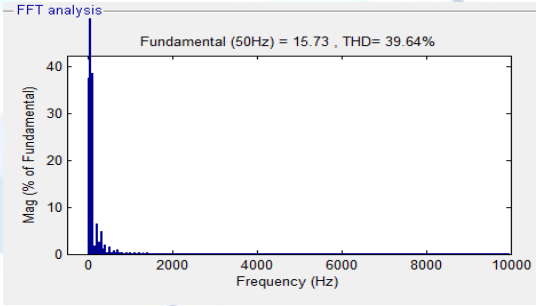

Fig.13 Branch current FFT analysis.

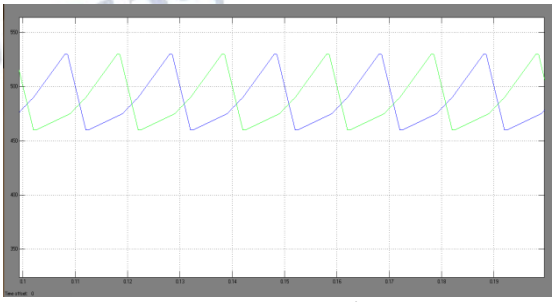

Fig.14 capacitor voltage.

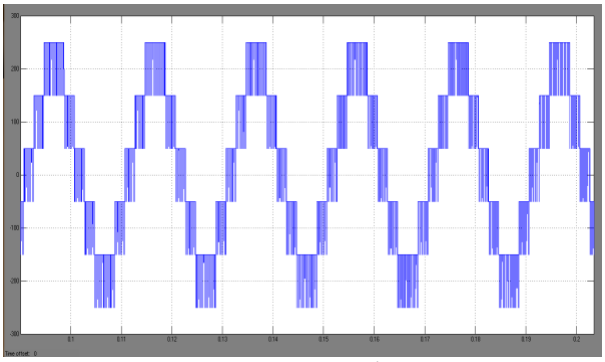

Fig.15 output ac voltages.

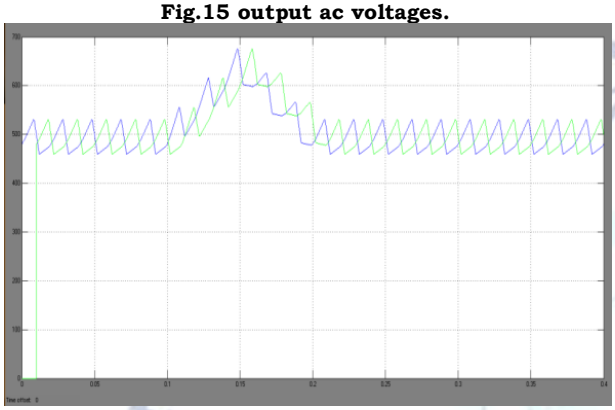

Fig.16. Capacitor voltage on dynamic test.

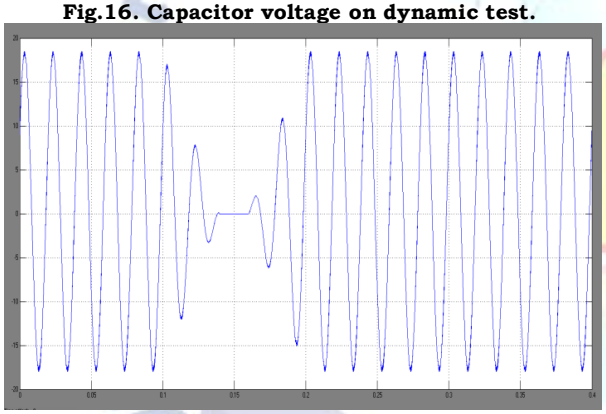

Fig.17. Load current on dynamic test.

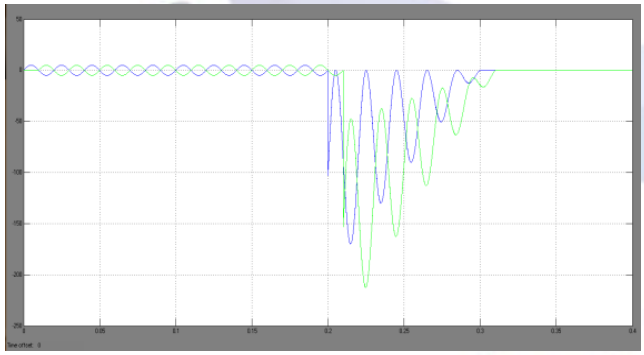

Fig.18. Branch current under line to line fault

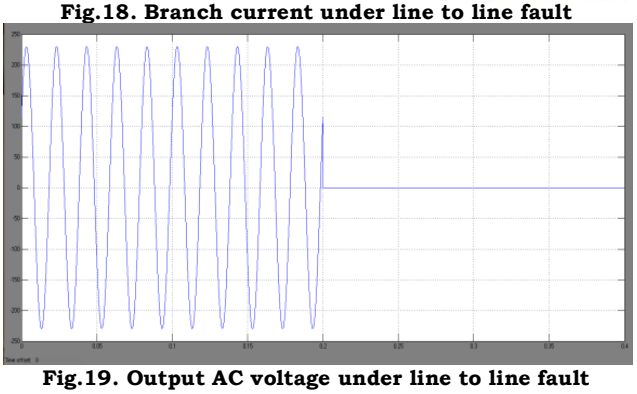

Fig.19. Output AC voltage under line to line fault

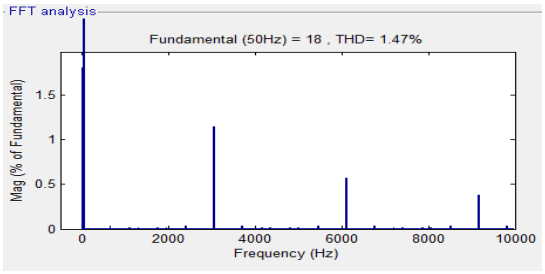

Fig.20 output current FFT analysis with PI controller

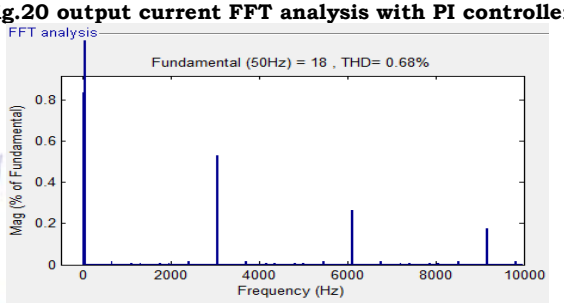

Fig.21 output current FFT analysis with Fuzzy logic controller.

IV. Conclusion

The design and performance study of the Modular Multi Level inverter with a fuzzy logic controller and an average current mode controller has been presented in this paper. It has been observed by both simulation and experimental verification that the use of sinusoidal multi carrier PWM technique with fuzzy logic control scheme incorporated with average current mode control scheme is promising in terms of reduction in terminal voltage harmonics and source current harmonics. The proposed work is aimed on the investigation of possible modeling and Fuzzy based control scheme for the VSC based HVDC transmission, with the purpose of identifying the impact of such modeling and control on the dynamics of the conversion system.

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