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Area Efficient Pulsed Clocks & Pulsed Latches on Shift Register Tanner

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ABSTRACT

This paper introduced a design and implementation of shift register using pulsed latches and flip-flops. As flip-flop based shift registers requires a clock signal to operate. Multistage flip-flop processes with high clock switching activity and then increases time latency. Flip-flops also engages fifty percent power out of total circuit power in clocking. To reduce such power consumptions and to achieve area optimization flip-flops are replaced by pulsed latches. The design is implemented with 250nm technology in Tanner EDA Tool. With Vdd=1.8V, Freq=100MHz. Average power of total circuit is 0.465uW and delay of 0.312 us.

KEYWORDS: *Flip-Flops, Area Efficient, Pulsed Clocks, Pulsed Latches, Shift Register, Tanner.*

I. INTRODUCTION

The rapid growth in semiconductor devices and VLSI designs has led to the development of high performance designs with enhanced reliability, customized size and low power, and because of the power dissipation is critical issue for battery operated systems. Therefore the designs are needed to be consuming less power while maintaining comparable performance. So everyone in VLSI design must think about area utilization and power dissipation. In low power digital design, mainly shift registers are designed using flip-flops of different types. To achieve area optimization and power consumption different techniques are introduced like use of double edge triggered flip-flip, single feed through scheme based flip-flop, use of multiple voltage supply, clock gating, voltage scaling etc. As it is a type of synchronous circuit all the flip-flops are clocked simultaneously. The flip-flop is basic data storage element. The operation of flip-flop is depending on clock frequency, which consumes 50% power out of total power in a digital design. At present, by decreasing CMOS technology process stated by Moore's law, more transistors can be integrated on the same die [1]. Applying more transistors is accompanied by more switching that brings out more energy dissipation in the form of heat and radiation [2].The heat and consistency of integrated circuits are addressed as important drivers of low power design procedures in RFID applications [3-7]. The packaging and cooling cannot remove additional heat, so the matter of heat is significant issue in the era [8]. FFs are addressed as fundamental storage element which is vastly finds application in all types of digital design [9].

Flip-Flop based shift registers are used in digital filters [10], image processing [11]. As the size of image data goes on increasing continuously, the demand of word size of shift registers also goes on increasing to process large image extraction 4K-bit [12].

The Shift registers are formed by cascade connection of flip-flops, sharing the same clock as it is a type of sequential circuit. That means the output of first flip-flop is given as the “Data” input of next flip-flop due to which shifting takes place. The speed of flip-flop is less important than area and power consumption because there is no any circuit between flip-flops in shift register. To reduce power and area smallest flip-flop is selected. Recently pulsed latches have been replaced the flip-flops in many applications, because latches are smaller than flip-flops. This paper proposes a design implementation of shift register using non overlapped pulsed latches, to achieve low power and area optimization. Latches cannot be used in

shift register design because of timing problem. The reminder of this paper is organized as follows. Section II presents problem statement. Section III presents Proposed Shift register. Section IV presents SSASPL working. Section V presents simulation designs. Section VI presents Conclusion. Section VII presents Experimental results.

II. Related Work

2.1 Complementary metal oxide semiconductor (cmos):

The MOSFET is used in digital complementary metal–oxide–semiconductor (CMOS) logic, which uses p- and n-channel MOSFETs as building blocks. Overheating is a major concern in integrated circuits since ever more transistors are packed into ever smaller chips. CMOS logic reduces power consumption because no current flows (ideally), and thus no power is consumed, except when the inputs to logic gates are being switched. CMOS accomplishes this current reduction by complementing every nMOSFET with a pMOSFET and connecting both gates and both drains together. A high voltage on the gates will cause the nMOSFET to conduct and the pMOSFET not to conduct and a low voltage on the gates causes the reverse. During the switching time as the voltage goes from one state to another, both MOSFETs will conduct briefly. This arrangement greatly reduces power consumption and heat generation. In this paper section II discuss about D flip flop and pulsed latch using CMOS and section III describes the CNTFET based D flip flop and pulsed latch. section IV describes the conclusion.

A. CMOS based SET D Flip Flop

SET D-flip flop is designed from power pc603 SET D-FF . The CMOS based flip flop design is shown in Fig.1.This flip-flop is a Master Slave flip flop structure and it consists of two data paths. As conventional n-type pass transistors give weak high output, but in this design the n-type pass transistors are followed by an inverter to give strong high output. Hence the SET D-Flip Flop is free from threshold voltage loss. Thus the designed Single Edge Triggered D-Flip-Flop has become more efficient in terms of area, power and speed and hence provides better performance than conventional Flip Flops.

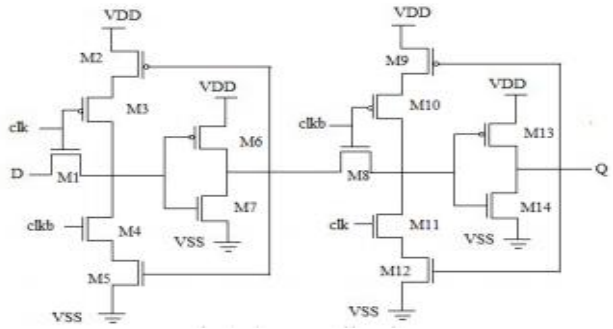


Fig 1. SET D Flip Flop.

B. CMOS based Pulsed Latch

CMOS is the most popular MOSFET technology. Here the SSASPL pulsed latch is realized using the CMOS logic which is shown in fig.2. The SSASPL consists of 15 transistors in which the transistors (M1-M8) are used to generate the pulsed clock signal and the transistors (M9-M15) are the schematic of SSASPL [15].

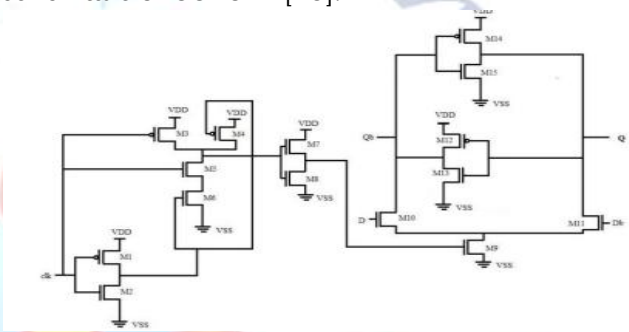


Fig. 2 CMOS based SSASPL

The pulsed clock signal generation circuit consists of AND gate, inverter and clock buffer. The clock signal is given to the inverter which inverts the signal and then the inverter output is given to one input of AND gate and another input is the clock signal which performs the AND operation. The output is given to the clock buffer which stores the data and given to the transistor M9 as the pulsed clock signal. The total size of the clock buffers is determined by the total clock loading of latches. The SSASPL updates the data with three NMOS transistors and it holds the data with four transistors in two cross-coupled inverters. It requires two differential data inputs (D and Db) and a pulsed clock signal. When the pulsed clock signal which is given to the gate of the transistor M9 is high, its data is updated. The node Q or Qb is pulled down to ground according to the input data (Dand Db). The pull-down current of the NMOS transistors must be larger than the pull-up current of the PMOS transistors in the inverters. The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading.

III. Implementation

3.1 CNTFET: carbon nano tube field effect transistor:

CNT is a carbon allotropic variety which comes from the fullerenes family. It is made of nano sized carbon atom and rolled in seamless cylindrical form of single atomic layered thick graphene sheet [4]. Fig. 3 (a) shows a CNT which is made from one sheet of graphene rolled in cylindrical structure which is called Single Wall Carbon Nanotube (SWCNT) and Fig. 3 (b) shows Multi Walled Carbon Nanotube (MWCNT) where multi-layers of graphene are rolled as

A concentric tube [5-7]. CNT based nano devices are comprised of wide range of nano structures. CNTFET could be used as valve or controlled switch in electronics. Carbon Nano Tube Field Effect Transistors for NEMS are emerging day byday not only in IC industry but also in medical science, mechanical system, automobile industry and recreational instruments [8].

Depending on their chirality (i.e., the direction in which the graphite sheet is rolled), the single-walled carbon nano tubes can either be metallic or semiconducting [9], [10]. CNFETs are one of the molecular devices that avoid most fundamental silicon transistor restriction and have ballistic or near ballistic transport in their channel [11],[12].Therefore a semiconductor carbon nanotube is appropriate for using as channel of field effect transistors [10]. Applied voltage to the gate can control the electrical conductance of the CNT by changing electron density in the channel. By using appropriate diameter suitable threshold voltage for CNFET can be achieved. The threshold voltage of the CNFET is proportional to the inverse of the diameter of CNT and can be expressed as:

A. Nanotube Geometry:

There are three unique geometries of carbon nanotubes. The three different geometries are also referred to as flavors. The three flavors are armchair, zig-zag, and chiral [e.g. zig-zag (n, 0); armchair (n, n); and chiral (n, m)]. These flavors can be classified by how the carbon sheet is wrapped into a tube is shown in Fig.4A1. Zigzag

The length L of the chiral vector Ch is directly related to the tubule diameter d. The chiral angle 0 between the Ch direction and the zigzag direction of the honeycomb lattice (n,O)[14]. The zig-zag model is the easiest one to count and the best one to try and copy when learning these geometries. Remember, our goal is to start and end at the same point. Hold the starting point between the finger and thumb of one hand (0,0) and use the other hand to count around the rolled up sheet and try to end where you begin. So, count each carbon atom around the tube - (1, 0) (2, 0) (3, 0) (4, 0) (5,0) etc., until you get back to the starting point. Once you have done this, you have just made a simple carbon nanotube model. The chiral angle in zigzag is zero.

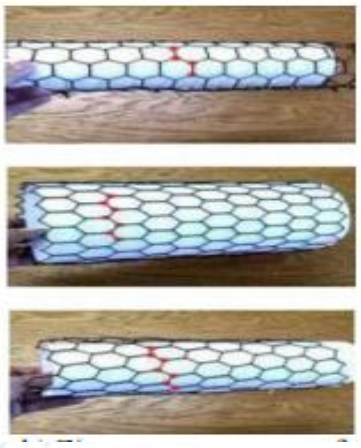


Fig.4 a)Armchair arrangement of carbon atoms b) Zig-zag arrangement of carbon atoms c) Chiral arrangement of carbonatoms.

B. Armchair

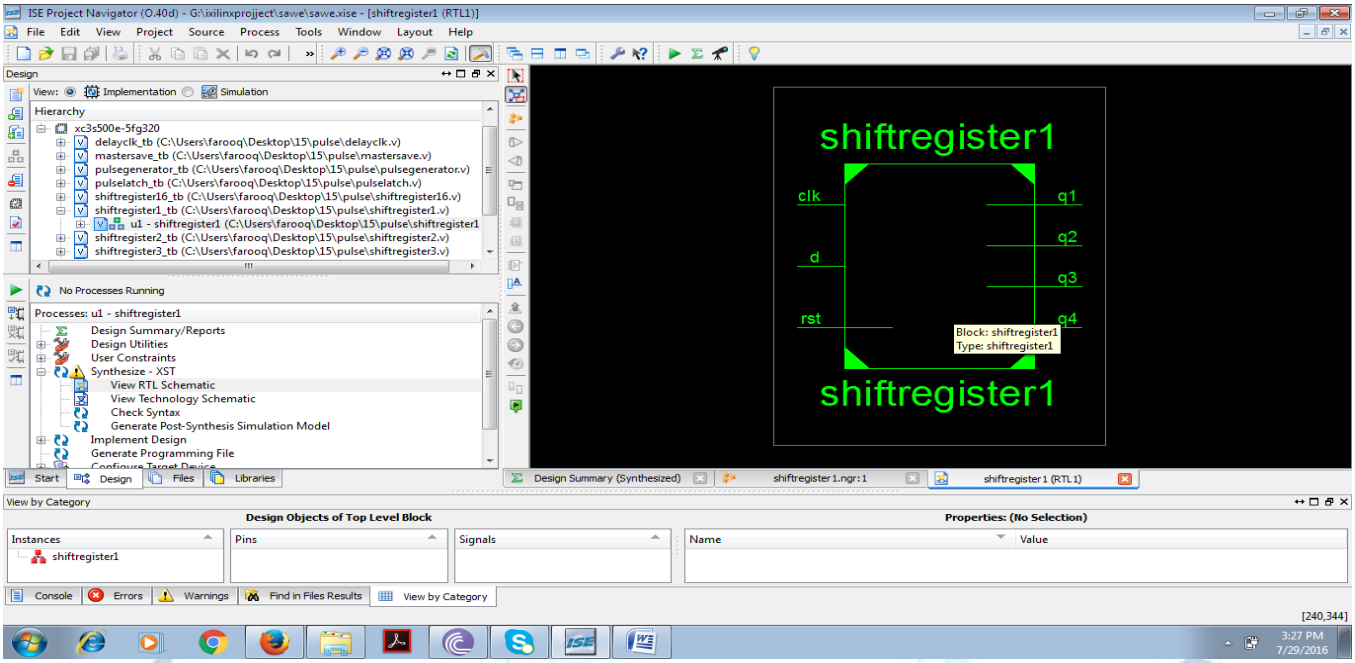
When you count around the tube, note that you are counting at an angle and it will not be possible to get back to your starting point unless you turn a corner. Note that you have to pick the right place to turn so that you end up at your starting point because you can only turn once. Again, count each carbon atom around the tube - (1, 0) (2, 0) (3, 0) (4, 0)(5, 0) until you get to a corner; after you turn, the count continues as - (5, 1) (5, 2) (5, 3) (5, 4) etc. - until you get back to the starting point. The chiral angle in armchair is 30 degree. A3. Charial

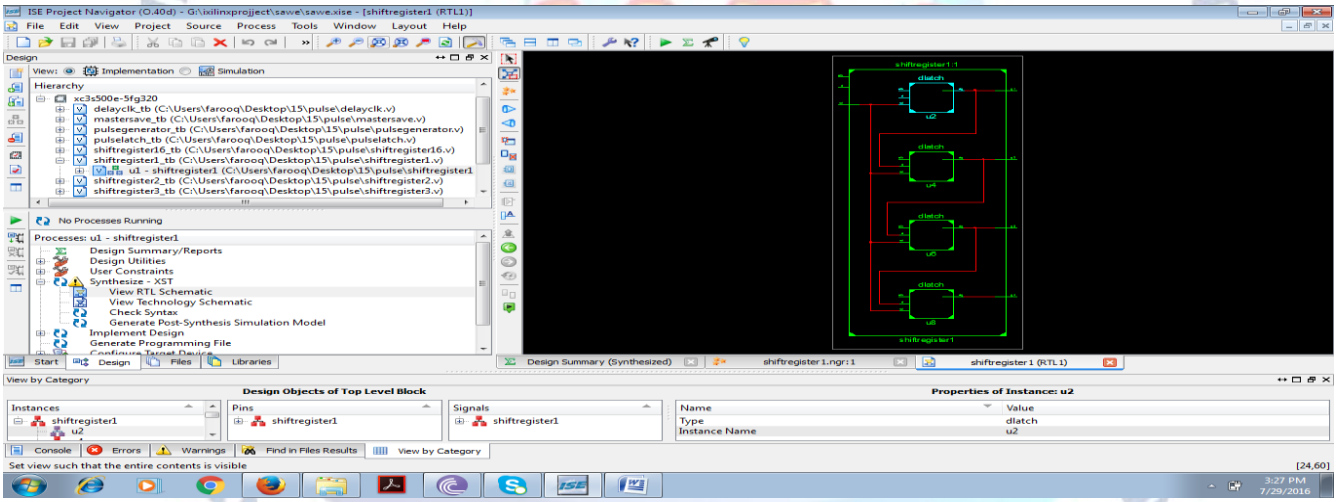
The last one is the chiral model. I think it is the most difficult to copy. It can be counted similarly like the arm chair model because it also has a turn it. Remember to try and end up where you start such that the charial angle fomed will be between 0 and 30 degree. The parameter of CNTFET is shown in the table I

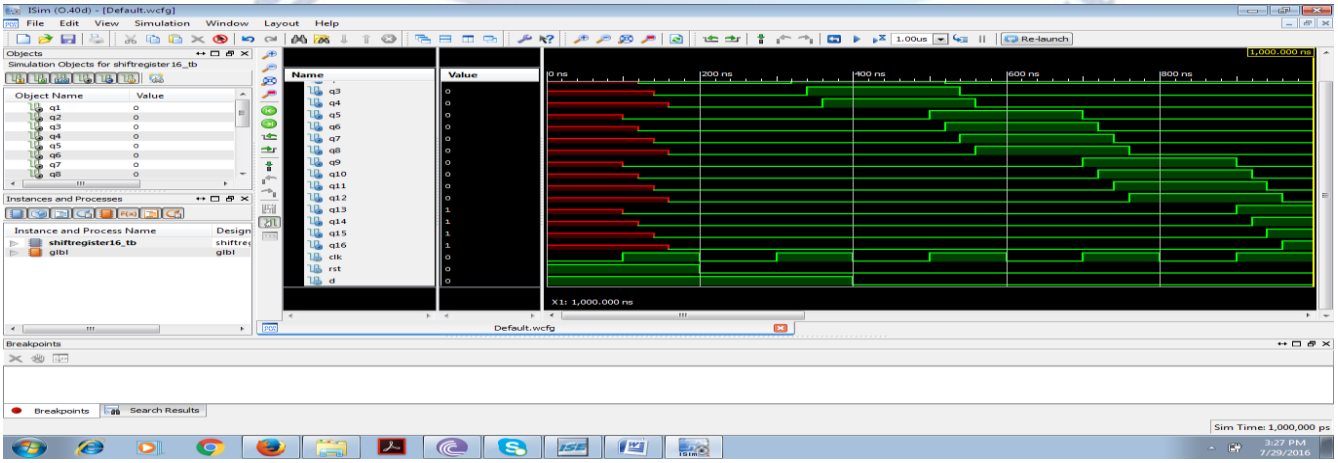
Parameter	Value
Supply Voltage (V_{DD})	1.0v
Physical channel length (L)	32nm
Diameter of the CNT (d)	1.487nm
The length of doped CNT source-side extension region. (L_{SS})	32nm
The length of doped CNT drain-side extension region.(L_{DD})	32nm
The thickness of high-k top gate dielectric material (T_{OX})	4nm
The dielectric constant of high-k top gate dielectric material (K_{OX})	16
The distance between the centers of two adjacent CNTs within the same device.	20nm
Chiral Vector	(19,0)

IV. EXPERIMENTAL WORK

Output Results are







V. Conclusion

This paper proposed a low-power and area-efficient shift register using digital pulsed latches. The shift register reduces area and power consumption by replacing flip flop switch pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal.

A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit shift register was fabricated using a 0.18µm CMOS process with VDD=1.8V. Its core area is 6600µm2. It consumes1.2 mW at a 100 MHz clock frequency. The proposed shift register saves 37% area and 44% power compared to the conventional shift register with flip-flops.

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