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Report on Ripple Carry Adder Power Delay using Brent Kung (BK) Adder

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ABSTRACT

In this paper, Carry Select Adder (CSA)architecture are proposed using parallel prefix adder. Instead of using 4-bit Ripple Carry Adder (RCA), parallel prefix adder i.e.,4-bit Brent Kung (BK) adder is used to design CSA. Adders are key element in digital design, performing not only addition operation, but also many other function such as subtraction, multiplication and division. Ripple Carry Adder (RCA) gives the most complicated design as-well-as longer computation time. The time critical application use Brent Kung parallel prefix adder to drive fast results but they lead to increase in area. Carry Select Adder understands between RCA and BK in term of area and delay. Delay of RCA is larger therefore we have replaced it with Brent Kung parallel prefix adder which gives fast result. Power and delay of 4-bit RCA and 4-bit BK adder architecture are calculated at different input voltage. This paper describes comparative performance of 4-bit RCA and 4-Bit BK parallel prefix adder designed using TANNER EDA tool.

KEYWORDS: *Brent Kung (BK) Adder, Ripple Carry Adder, Power, Delay.*

I. INTRODUCTION

In this paper, describe demand for high-speed arithmetic units in digital image processing units, DSP and other processor chips has superimpose the path for develop of high speed adders as addition is an essential operation in almost every arithmetic unit, also the basic building block for combination of all other arithmetic logical computations .To increase portability of systems and battery life, delay and power are the ensuring the success of concern. Even in servers and personal computers (PC), power efficient is a vital design parameter. In now day's scenario, Design of power-efficient high-speed logic systems in VLSI design techniques. In digital adders, the speed of addition is limited time required by the carry to generate through the adder. In present scenario, where Computations need to be performed using low-power circuit that must operate at high speed which is achievable with lesser delay that's why this paper describes comparative performance of 4-bit RCA and 4-Bit BK parallel prefix adder designed using TANNER EDA tool. Finally delay, power for the design adder presented and compare.

A. Drawbacks of Ripple Carry Adder

Multiple full adder circuits can be rapidly cascaded in parallel to addition of N-bit number. For an N- bit cascaded parallel adder, there must be N number of full adder circuits[1]. A ripple carry adder is a logic circuit in which the carry out of each full adder parameter is the carry in of the following next most significant full adder. It is called a ripple carry adder because each and every carry bit gets wind up into the next stage of adder. In figure1, the first sum bit should wait up until input carry is given; the second sum bit should wait up until previously carry is propagated and so on. Finally the output sum should wait up until all previous carries are generated. So it results in delay.

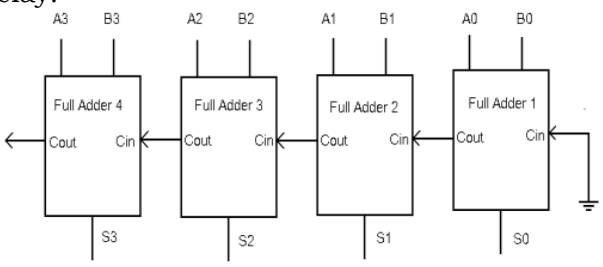

Fig 1. 4-bit ripple carry adder.

II. Related Work

A. Parallel Prefix Adders

These are used to take the binary additions because of their flexibility. Carry Look Ahead Adder's (CLA) structure is utilized in order to get the parallel prefix adders. Tree structures algorithm are used to increase the speed high performance of arithmetic operation. Parallel prefix adders are used for high performance arithmetic circuits in industries as they increase the speed of operation. The construction of parallel prefix Adder involves three stages:

1. Pre- processing stage
2. Carry generation Process
3. Post processing stage

Pre-possessing stage:-

Generate and propagate signals to each pair of the inputs A and B are computed in this stage. These signals are given by the,

Following equations:

Pi=Ai xor Bi (1)

Gi=Ai and Bi (2)

Carry generation network:-

In this stage, carries equivalent to each bit is calculated. All these operations are implemented and carried out in parallel. Carries in parallel are segmented into smaller pieces after the implementation of the stage. Carry propagate and generate are used as intermediate signals which are given by the logic equations3& 4:

CPi:j=Pi:k+1 and Pk:j (3)

CGi:j=Gi:k+1 or (Pi:k+1 and Gk:j) (4)

The operations involved in fig. 1 are given as:

CPO=Pi and Pj (3(i))

CGO=(Pi and Gj) or Gi (3(ii))

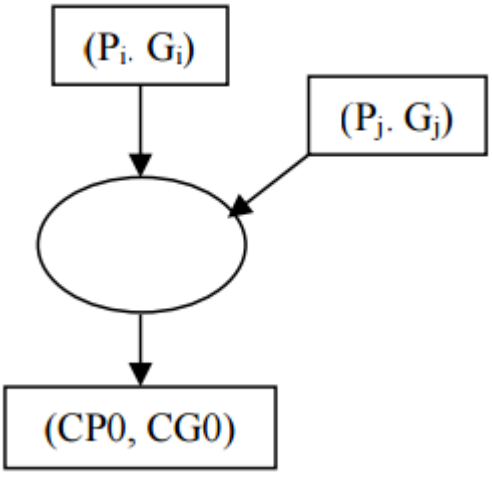

Fig 2. Carry Network.

Post processing Stage:-

This is the concluding step to compute the summation of input bits. It is similar for all the adders and then sum bits are computed by logic operation equation 4& 5:

Ci-1= (Pi and Cin) or (4)

Si=Pi xor Ci-1 (5)

Brent-Kung Adder:-

Brent-Kung adder is a very popular and widely used adder. It actually gives an excellent number of stages from input to all outputs but with asymmetric loading of Intermediate stages. It is one of the parallel prefix adders. It is one of the parallel prefix adders where these adders are the ultimate class of adders that are based on the use of generate and propagate signals. In case of Brent Kung adders along with the cost, the wiring complexity is also less. But the gate level depth of Brent-Kung adders is 0 (log2 (n)), so the speed is lower. The block diagram of 4-bit Brent-Kung adder is shown in Fig. 3.

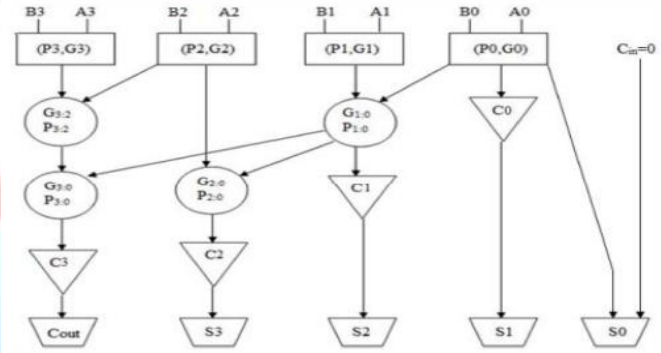

Fig 3. Tree Diagram of 4-bit Brent Kung Adder.

III. Implementation

A. 4-Bit Ripple Carry Adder

This fig. 4 has CMOS Ripple-carry select adders are the simplest and most compact full adders, but their concert is limited by a carry that must propagate from the least -significant bit to the most- significant bit Ripple Carry Adder(RCA) gives the most compact design as-well-as longer computation time.

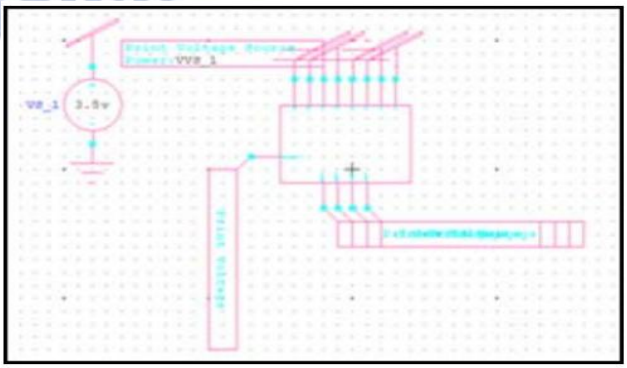

Fig 4. 4-BIT RCA Schematic.

Figure 5 is the output waveform for 4 bit RSA structure. Input is varied from 0000 to 1111 and corresponding output is observed at each instant of time. Waveform is seen in W-edit window of tanner

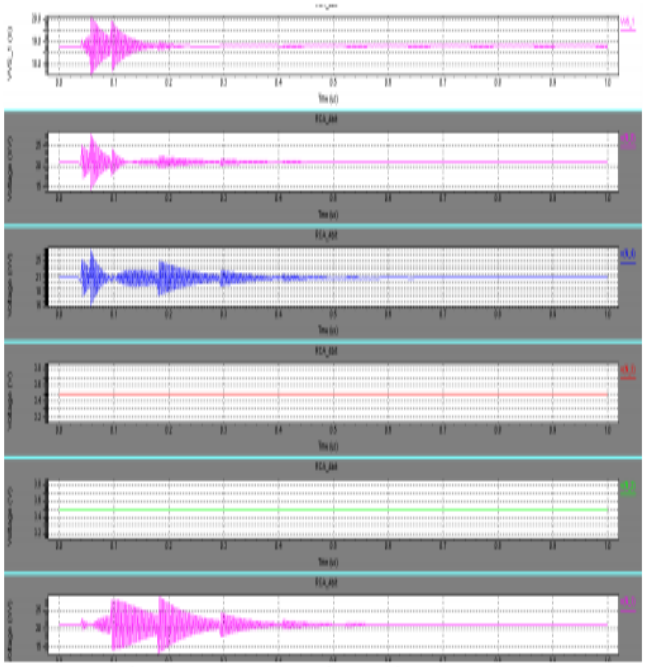

Fig 5. Output Waveform of 4-BIT RCA.

IV. Experimental Work

Various adders were designed in Tanner EDA version 13.0tool using CMOS technology. Power consumption and delay of Ripple Carry Adder and Brent Kung prefix adder 4-Bitword size. The comparison of various adders for different parameters like delay and power consumption is shown in Table I. The result analysis shows that Brent Kung Carry Select Adder shows better results than the Ripple carry adder architectures in terms transient analysis of delay and high speed at different input voltages but with a small power penalty. The graphical representation of comparison of RCA and BK CSA for different input voltages for power and delay consumption is shown in fig. Results show BK CSA better results than RCA.

Table I. Comparison of RCA and BK-CSA Adders for transient Delay at Various Input Voltages.

Adder	Supply Voltage Transient Delay(sec)				
	3V	3.5V	4V	4.5V	5V
4-Bit RCA	1.23	1.30	0.95	2.31	0.94
4-Bit BK CSA	0.20	0.20	0.16	0.16	0.19

Figure 8 is the graphical representation of comparison of RCA and BK CSA at different input voltages for transient Delay is shown in fig. Results show that BK CSA strongly high speed results than RCA.

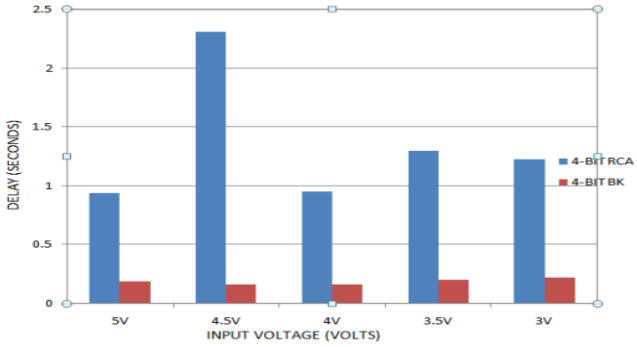

Fig 8. Comparison of RCA and BK CSA Adders for Transient Delay at Various Input Voltages.

Figure 9 is the graphical representation of comparison of RCA and BK CSA at different input voltages for power consumption is shown in fig. Results show that RCA slightly better results than BK CSA.

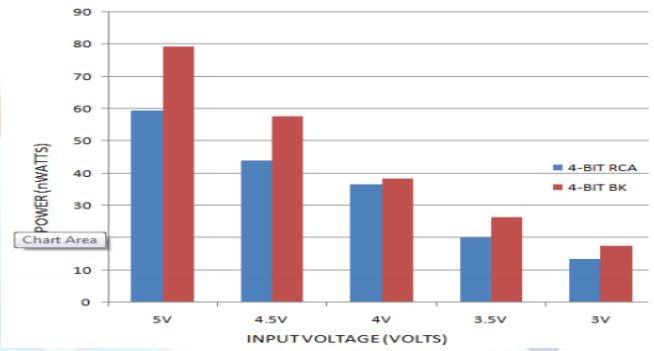

Fig 9. Comparison of RCA and BK CSA Adders for Power at Various Input Voltages.

V. Conclusion

This work can be extended for higher number of bits also. By using parallel prefix adder, delay and power consumption of different adder architectures is reduced. As, parallel prefix adders derive fast results therefore Brent Kung adder is used. The calculated results conclude that BK Carry Select Adder is better in terms of power consumption and high speed when compared with RCA adder architectures and can be used indifferent applications of adders like in multipliers, to execute different algorithms of Digital Signal Processing like Finite Impulse Response, Infinite Impulse Response etc.

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